Metal oxide-graphene field-effect transistor: interface trap density extraction model

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Full Research Paper

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Abstract

A simple to implement model is presented to extract interface trap density of graphene field effect transistors. The presence of interface trap states detrimentally affects the device drain current–gate voltage relationship I_{ds}–V_{gs}. At the moment, there is no analytical method available to extract the interface trap distribution of metal-oxide-graphene field effect transistor (MOGFET) devices. The model presented here extracts the interface trap distribution of MOGFET devices making use of available experimental capacitance–gate voltage C_{tot}–V_{gs} data and a basic set of equations used to define the device physics of MOGFET devices. The model was used to extract the interface trap distribution of 2 experimental devices. Device parameters calculated using the extracted interface trap distribution from the model, including surface potential, interface trap charge and interface trap capacitance compared very well with their respective experimental counterparts. The model enables accurate calculation of the surface potential affected by trap charge. Other models ignore the effect of trap charge and only calculate the ideal surface potential. Such ideal surface potential when used in a surface potential based drain current model will result in an inaccurate prediction of the drain current. Accurate calculation of surface potential that can later be used in drain current model is highlighted as a major advantage of the model.

Introduction

Graphene has recently attracted a lot of attention. Its 2D nature along with its significantly high carrier mobility (≈15,000 cm^2/(V·s)) make it an ideal material to replace silicon [1] in the more than Moore era. During deposition of the dielectric layer on graphene as well as from deposition of graphene on the substrate defects may be formed in the film resulting in the

presence of trap states; D_{it} states (cm^{-2}·eV^{-1}) at the interface between the dielectric layer and graphene channel [2,3]. These trap states trap mobile carriers degrading the gate field modulation effect, thereby resulting in degraded surface potential.

Popular metal-oxide-graphene field-effect transistor (MOGFET) models do not take into account the detrimental effect of D_{it} states on device surface potential [4,5]. Zebrev et al. [6], recently presented a model that takes into account the effect of D_{it} states on the device current. A similar approach has been used by [7]. However, Zebrev's drain current expression is based on the assumption of presence of constant D_{it} states over the entire energy range of operation of the device. The assumption does not work generally; recently, significantly varying D_{it} distribution has been reported for metal-oxide-graphene (MOG) capacitors [8]. This suggests the need for a model that can analytically calculate the interface trap density of MOGFET devices that could later be used in drain current I_{ds} models for efficient I_{ds} performance prediction.

This work presents a method to extract interface trap density of MOGFET with the help of device C_{tot}–V_{gs} data. Basic equations and parameters needed to extract interface trap density are explained below. Extraction and verification of extracted trap density is explained following the section below.

Basic equations and parameters
Basic equations
Figure 1a shows the schematic of a typical MOGFET. The channel consists of monolayer graphene with length L deposited on a SiO$_2$ layer with a p-type doped silicon substrate as the backgate (only top-gated monolayer MOGFET is considered in this work). The gate stack consists of a dielectric layer with thickness t_{ox} and a metal gate. Q_{it} in Figure 1a refers to the interface trap charge found at the dielectric/channel interface. Figure 1b shows the equivalent capacitive circuit of the typical capacitances in the MOGFET device. In a MOGFET top gate capacitance C_{ox} is in series with the parallel combination of interface trap capacitance C_{it} which originates from the presence of D_{it} states, and C_q the quantum capacitance.

C_q is a graphene material property and is given by [9],

$$C_q = \sqrt{C_{qi}^2 + (\beta_g q \varphi_s)^2}. \tag{1}$$

where, q is the charge on an electron, φ_s is surface potential,

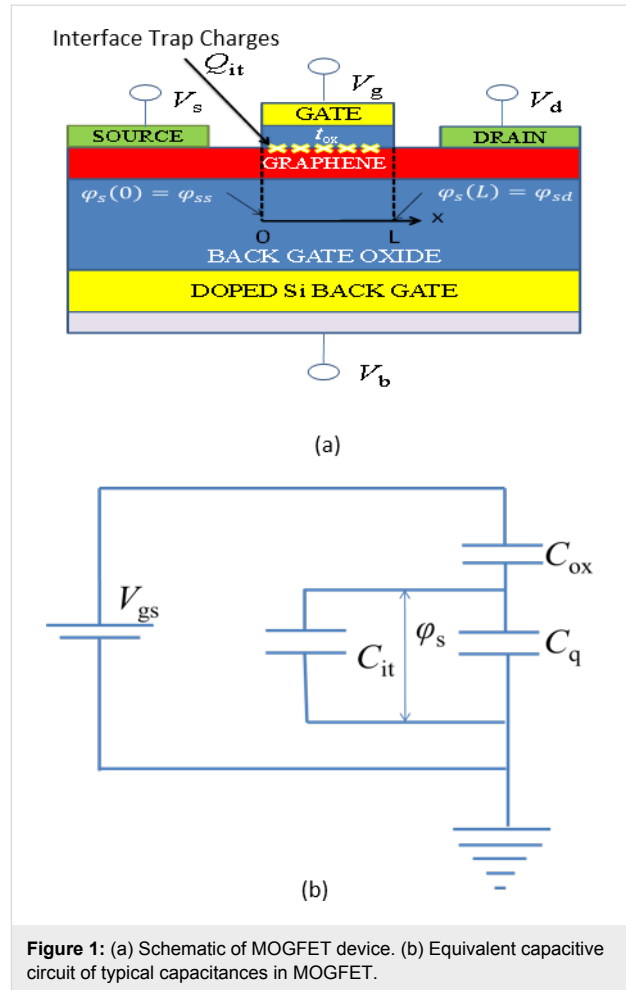$$\beta_g = \frac{2q^2}{\pi \hbar^2 v_f^2}, $$

Figure 1: (a) Schematic of MOGFET device. (b) Equivalent capacitive circuit of typical capacitances in MOGFET.

$\hbar$ is the Planck's constant, v_f is the fermi velocity (1×10^8 cm^2/(V·s)), C_{qi} is a fitting factor independent of φ_s, and accounts for the finite C_q observed at Dirac point (DP) (at which the fermi level $E_f = q\varphi_s = 0 = E_D$, where E_D is the energy (eV) at DP).

The total capacitance C_{tot} of MOGFET is given by,

$$C_{tot} = \frac{C_{ox}\left(C_q + C_{it}\right)}{C_{ox} + C_q + C_{it}}. \tag{2}$$

Applying the capacitor divider relation to Figure 1b, the surface potential φ_s of MOGFET is given by,

$$\varphi_s = \frac{(V_{gs} - V_{DP} - V_c)C_{ox}}{C_{ox} + C_q + C_{it}}, \tag{3}$$

where V_{gs} is the gate voltage, V_{DP} is the gate voltage at DP known to be caused by the gate-metal/graphene workfunction

difference [10], and/or interface trap states [11], and V_c is the channel voltage drop due to the applied drain bias V_{ds} with $V_c = 0$ at the source end and $V_c = V_{ds}$ at the drain end.

Solving self-consistently for φ_s in Equation 3 and $C_q = (\beta_g q \varphi_s)$, φ_s is given by Equation 4,

$$\varphi_s = \frac{-\left(C_{ox} + C_{it}\right)}{\pm 2\beta_g q} + \frac{\sqrt{\left(C_{ox} + C_{it}\right)^2 \pm 4\beta_g q \left(V_{gs} - V_{DP} - V_C\right) C_{ox}}}{\pm 2\beta_g q} \tag{4}$$

Here, the positive (negative) sign applies when $(V_{gs} - V_{DP} - V_c)$ $C_{ox} > 0$ (< 0). The sum of $C_q + C_{it}$ in Equation 2 and Equation 3 can be labeled as C_x. The next few paragraphs explain the procedure for extraction of experimental φ_s, C_q, C_{it} and Q_{it} parameters of two sample MOGFET devices which are then used in extraction of their D_{it} distributions explained in the section "Extraction of interface trap states".

Experimental φ_s, C_{it}, and Q_{it} extraction

Surface potential φ_s and C_{it} were extracted for two MOGFET devices using experimental $C_{tot}–V_{gs}$ data (from herein referred as C_{tot_exp}) taken from Device 1 [7], and device 2 [12] (with back-gate bias = 0 V, and $V_{ds} = 0$). The extracted φ_s and C_{it} parameters obtained using experimental C_{tot_exp} data will be referred to as φ_{s_exp} and C_{it_exp}. The device parameters for both the devices are mentioned in Table 1.

Table 1: Device parameters for devices 1 and 2.

Device	Device parameter	MOGFET reported/used value
Device 1 [7]	C_{ox} (µF/cm²)	1.98
	V_{DP} (V)	0.2
	C_{qi} (µF/cm²)	1
Device 2 [12]	C_{ox} (µF/cm²)	0.76
	V_{DP} (V)	0.11
	C_{qi} (µF/cm²)	1.6

As mentioned in [12] for Device 2, the DC method used to find C_{ox} involves a large amount of ambiguity due to imprecise evaluation of the back-gate capacitance [13], and consequently C_{ox}. A C_{ox} value of 1.00 µF/cm² along with available C_q and C_{it} parameters from [12] in Equation 2 was found to reproduce available C_{tot_exp}, and C_q results very well, instead of the reported value of 0.76 µF/cm², the former is used instead in this work. The extraction procedure is described next.

C_x can be found from Equation 5 which is derived from manipulating Equation 2. Here C_{tot} is the respective experimental $C_{tot}–V_{gs}$ data for the two experimental devices and C_{ox} is their oxide capacitances mentioned in Table 1.

$$C_x = \frac{C_{ox} C_{tot}}{C_{ox} - C_{tot}} \tag{5}$$

C_x obtained from the above equation is then substituted in Equation 3 to extract device's φ_s as a function of V_{gs}, with all the other parameters in Equation 3 known. The extracted φ_s is referred to as φ_{s_exp} as device's surface potential extracted from experimental $C_{tot}–V_{gs}$ data.

Once φ_{s_exp} is obtained, C_q can be calculated from Equation 1. Finally, device's C_{it} can be obtained using the expression below. The extracted C_{it} is referred to as C_{it_exp} as device's interface trap capacitance obtained from experimental $C_{tot}–V_{gs}$ data.

$$C_{it\_exp} = C_x - C_q \tag{6}$$

By substituting C_{it_exp} in the expression given below, device's Q_{it} can be extracted.

$$Q_{it\_exp} = \frac{1}{q} \int_{E_D}^{E_f} C_{it\_exp} dE_f \tag{7}$$

In Equation 7 $E_f = \varphi_{s\_exp}$. The extracted Q_{it} is referred to as Q_{it_exp} as the interface trap charge extracted from experimental $C_{tot}–V_{gs}$ data.

The relationship between C_{it} and Q_{it} is given by

$$C_{it} = \frac{dQ_{it}}{d\varphi_s}. \tag{8}$$

Extraction of interface trap states

For the extraction, according to standard convention [6] acceptor and donor type traps states were considered for the n-type MOGFET, and p-type MOGFET operation, respectively.

The interface trap charge for both acceptor type and donor type trap states can be calculated from the following [11],

$$Q_{it\_calc} = q \int_{E_D}^{E_f} D_{it}(i) F_{tA(D)}(i) dE_f \tag{9}$$

$$F_{tA(i)} = \frac{1}{1 + \exp\left(E_{tA(i)} - E_f\right) / k_B T} \tag{10}$$

$$F_{tD(i)} = 1 - \frac{1}{1 + \exp\left(E_{tD(i)} - E_f\right)\big/k_B T} \qquad (11)$$

Here, in Equation 9–11, Q_{it_calc} denotes the calculated interface trap charge, F_{tA} (F_{tD}) denotes the probability of occupation of k acceptor (donor) type trap states, and E_{tA} (E_{tD}) denotes the ith energy level of each of these k acceptor (donor) type trap state. D_{it} is the interface trap density defined at the ith energy level. Q_{it} can be found by the integral of product of all the k trap states with their respective F_{tA} (F_{tD}) between E_D and E_f.

D_{it} distribution extraction criteria are based on our earlier work on MoS$_2$ MOSFET [14], and are highlighted in Figure 2. The following procedure describes D_{it} extraction criteria for MOGFET devices using the two reference experimental devices. As a first step, Q_{it_exp} and φ_{s_exp} values are extracted using the procedure outlined in the previous section. Next, the extracted φ_{s_exp} is substituted in Equation 10 and Equation 11 as $E_f = q\varphi_{s\_exp}$ to calculate $F_{tA(D)}$ values. These $F_{tA(D)}$ values are then used in Equation 9 to find Q_{it_calc}. In this step and the step prior to this, D_{it} values in Equation 9 and $E_{tA(D)}$ values in Equation 10 and Equation 11 are fitted for each energy level such that Q_{it_calc} obtained using this procedure matches, as a function of φ_{s_exp}, experimental Q_{it_exp} extracted earlier. This is indicated by step 3 of the flowchart shown in Figure 2.

If Q_{it_exp} and Q_{it_calc} values as a function of φ_{s_exp} match it means the fitted D_{it} values used in Equation 9 to calculate Q_{it_calc} were a good fit to reproduce the extracted experimental Q_{it_exp}. This step enables us to calculate D_{it} values.

At this point, we have only calculated Q_{it_calc} as a function of φ_{s_exp}. In order to compare parameters consistently we need to self-consistently find Q_{it_calc} as a function of φ_{s_calc}, where φ_{s_calc} refers to φ_s calculated from Equation 4 using C_{it_calc} as the input variable. C_{it_calc} refers to C_{it} calculated from Equation 8 using Q_{it_calc} and φ_{s_calc} as input variables. The self-consistent C_{it_calc}–φ_{s_calc} calculation procedure is based on our earlier works on MOSFET interface trap drain current modeling [14,15]. The procedure is highlighted in Figure 3 and is described next.

The first step is calculating C_{it_calc} from Equation 8 by substituting Q_{it_calc} obtained in the previous step (i.e., during the D_{it} extraction procedure) and the earlier obtained φ_{s_exp}. The calculated C_{it} is referred to as C_{it_calc}. Calcuted C_{it_calc} is then substituted in Equation 4 to find φ_{s_calc}. This φ_{s_calc} is then substituted back in Equation 9–11 using the already extracted interface trap distribution to calculate Q_{it_calc}. This Q_{it_calc} along with φ_{s_calc} obtained in the previous step is substituted back in Equation 8 to find C_{it_calc} which is then substituted in Equation 4 to find φ_{s_calc}. This process is repeated back and forth until self-consistency is obtained between Q_{it_calc}/C_{it_calc}
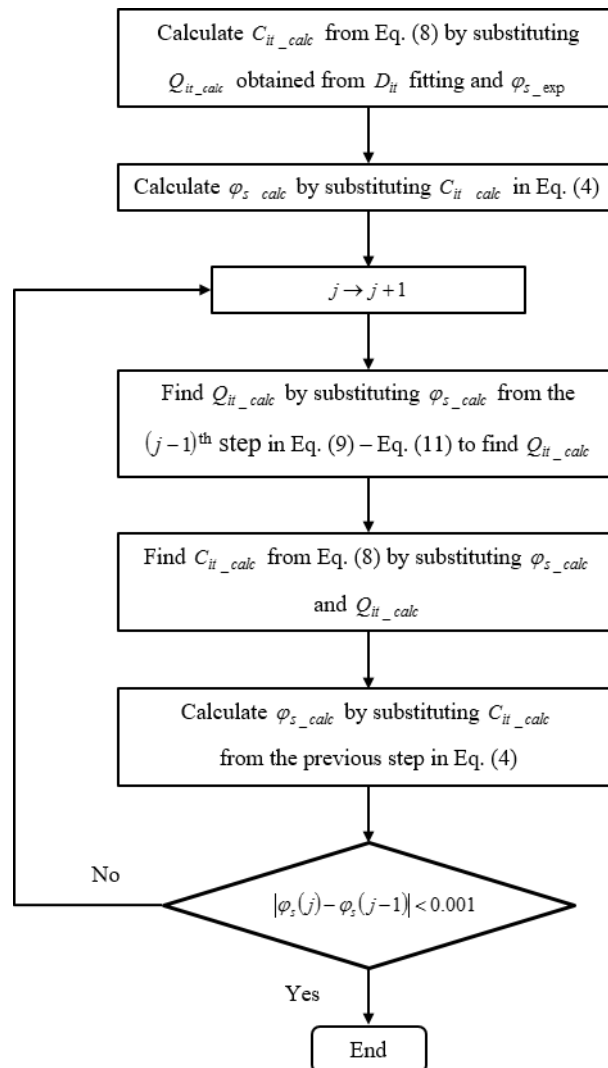

Figure 2: D_{it} distribution extraction procedure.
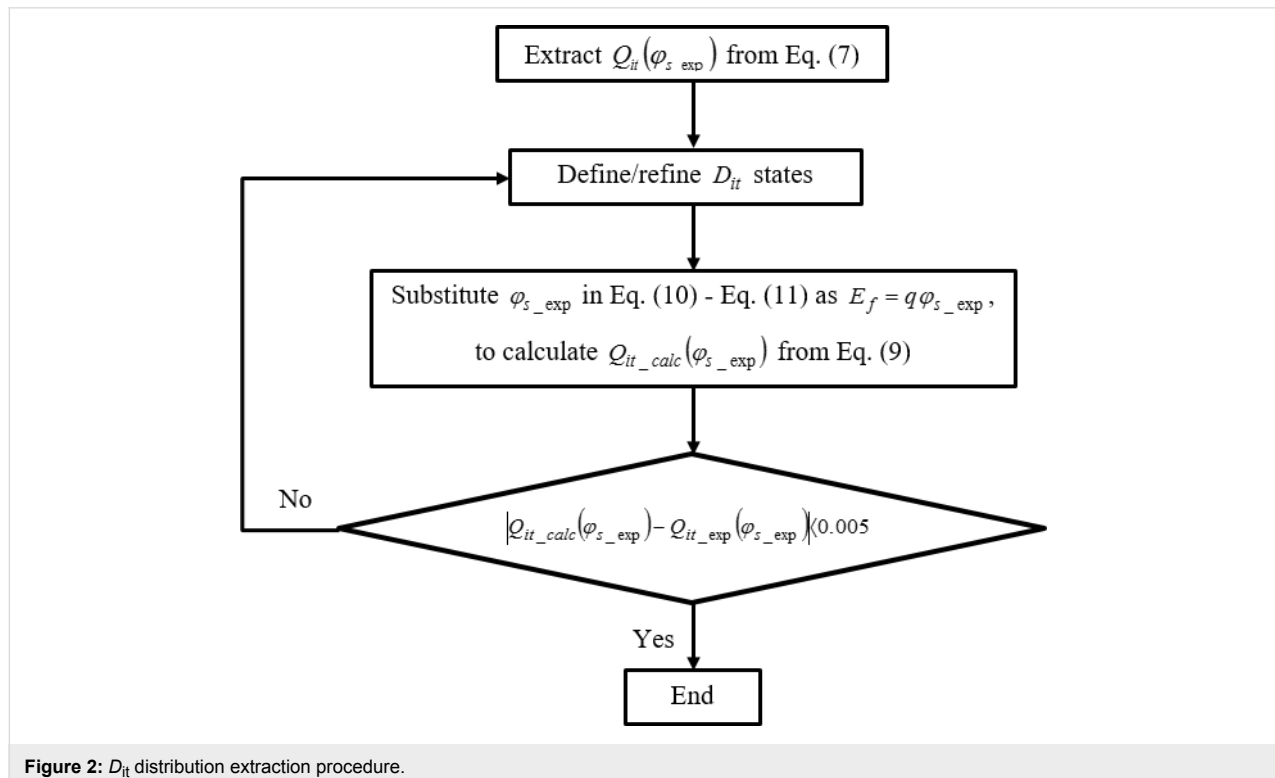
Figure 3: $\varphi_{s\_calc}/Q_{it\_calc}$ self-consistent calculation procedure.

and φ_{s_calc}. Now we can express Q_{it_calc}/C_{it_calc} as functions of φ_{s_calc}, and in turn φ_{s_calc} is calculated using C_{it_calc}.

Interface trap distribution verification criteria simply implies that

1. Q_{it_calc} (as a function of φ_{s_calc}) should match well with Q_{it_exp} (as a function of φ_{s_exp}).
2. C_{it_calc} (as a function of φ_{s_calc}) should match well with C_{it_exp} (as a function of φ_{s_exp}).
3. φ_{s_calc} should match well with φ_{s_exp}.

If the respective calculated and experimental parameters are in reasonable agreement, it proves that the fitted D_{it} values used to find the calculated parameters were reasonable (within a toler-

ance limit) to match well the experimental parameters. The extracted D_{it} distribution is shown in Figure 4; magenta for Device 1 and yellow for Device 2.

Results and Discussion

To prove the validity of the extraction criteria, the extracted experimental parameters, i.e., Q_{it_exp}, C_{it_exp}, φ_{s_exp}, and C_{tot_exp} are compared with the respective calculated, i.e., Q_{it_calc}, C_{it_calc}, φ_{s_calc}, and C_{tot_calc} parameters obtained using the extracted D_{it} distribution, as shown in the following.

Figure 5a and 5b compare for Device 1 and 2, respectively, the extracted Q_{it_exp} from Equation 7 (symbols) as a function of φ_{s_exp} with the self-consistently calculated Q_{it_calc} as a function of φ_{s_calc}. Q_{it_exp}, and Q_{it_calc} are in reasonable agreement
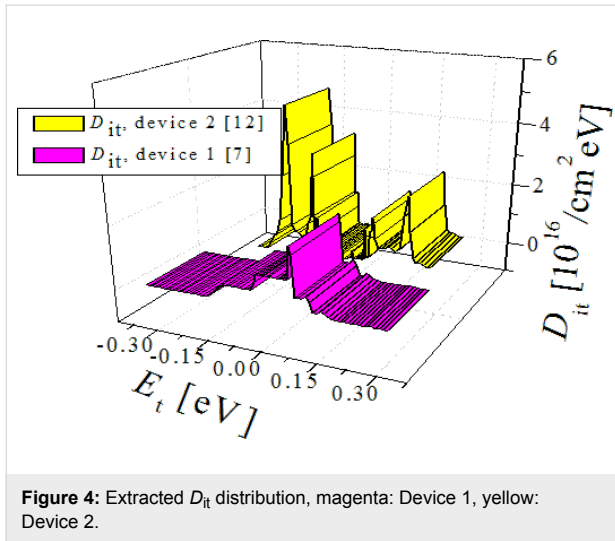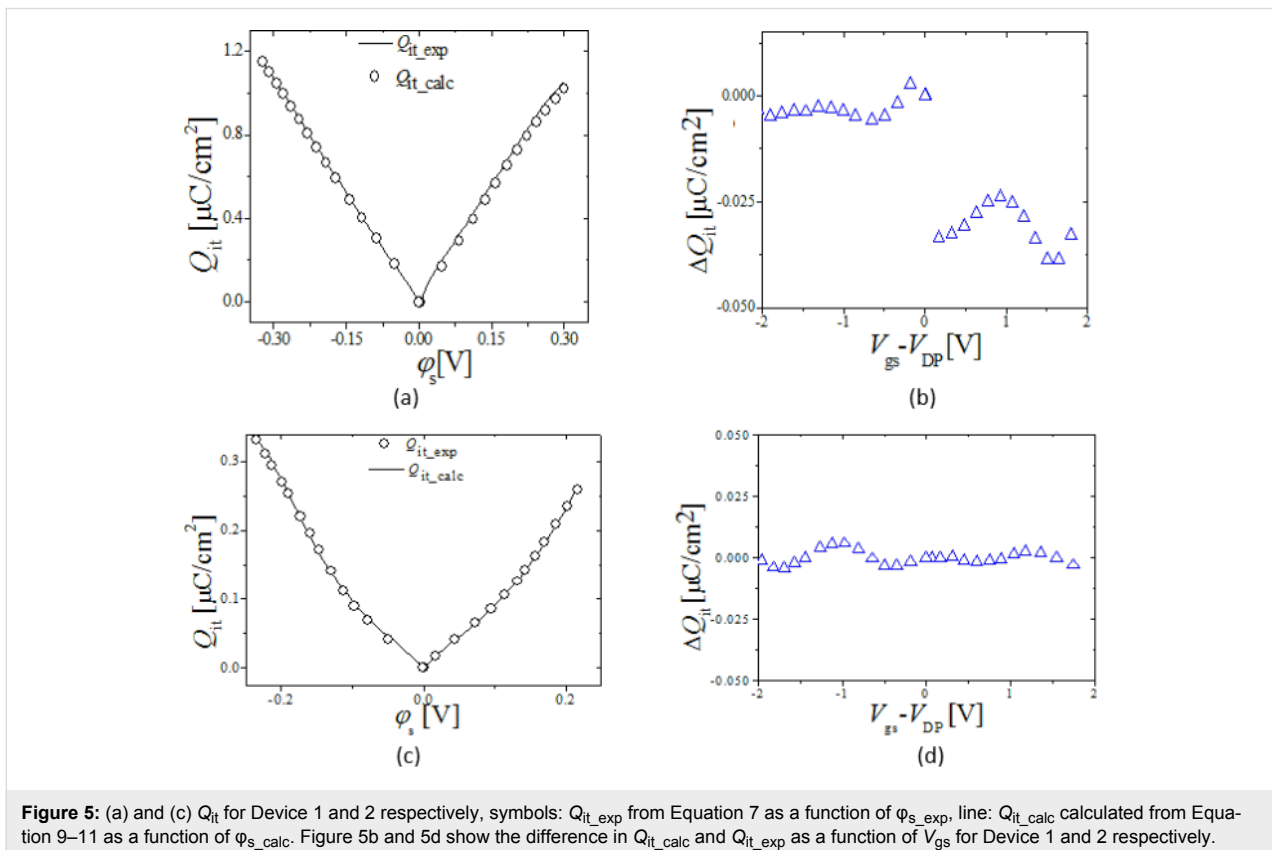
Figure 4: Extracted D_{it} distribution, magenta: Device 1, yellow: Device 2.

Also shown is φ_s-ideal, calculated from Equation 4 with $C_{it} = 0$ (dashed line). The surface potential calculated with no $C_{it} = 0$ compared with the surface potential calculated considering C_{it} clearly indicates that with no C_{it} included in the surface potential calculation the result will be an erroneously calculated surface potential. Such an erroneous surface potential if used in surface potential based drain current models will lead to unrealistic prediction of device current. Blue symbols in Figure 6a and 6b show the difference in φ_{s_exp} and φ_{s_calc}. As the graph shows, the difference between the two is minimal. The model ensures accurate, realistic calculation of device surface potential by taking into account degradation caused by trap states. This feature could be used to develop more realistic drain current models.

Figure 7a and 7b show for Device 1 and 2 respectively, the extracted C_{it_exp} (symbols) from Equation 6, as a function of φ_{s_exp} compared with the C_{it_calc} (solid line), as a function of φ_{s_calc}; C_{it_exp} is in reasonable agreement with C_{it_calc}. Figure 7b and 7d show difference in C_{it_exp} and C_{it_calc} as a function of V_{gs}. The error in C_{it_calc} although, higher than Q_{it_calc} is still negligible. This is proven when we substitute C_{it_calc} in Equation 4 to calculate φ_{s_calc} (when self-consistency is obtained), φ_{s_calc} matches very well with φ_{s_exp} as shown earlier in Figure 6.

as shown by Figure 5b and 5d which show the difference in Q_{it_calc} and Q_{it_exp} as a function of V_{gs}, for Device 1 and 2, respectively.

Figure 6a and 6b show for Device 1 and 2, respectively, the extracted φ_{s_exp} (symbols) as a function of $V_{gs} - V_{DP}$ compared with φ_{s_calc} (solid line) as a function of $V_{gs} - V_{DP}$; φ_{s_exp} is in excellent agreement with φ_{s_calc}.

Figure 5: (a) and (c) Q_{it} for Device 1 and 2 respectively, symbols: Q_{it_exp} from Equation 7 as a function of φ_{s_exp}, line: Q_{it_calc} calculated from Equation 9–11 as a function of φ_{s_calc}. Figure 5b and 5d show the difference in Q_{it_calc} and Q_{it_exp} as a function of V_{gs} for Device 1 and 2 respectively.

Figure 6: (a) and (b) φ_s for Device 1 and 2 respectively as a function of V_{gs}, symbols: extracted φ_{s_exp}, lines: φ_{s_calc} calculated from Equation 4 using the self-consistently obtained C_{it_calc}/Q_{it_calc} from Equation 8–11, dashed lines; φ_{s_calc}-ideal from Equation 4 with $C_{it} = 0$. Blue symbols show the difference in φ_{s_calc} and φ_{s_exp}.
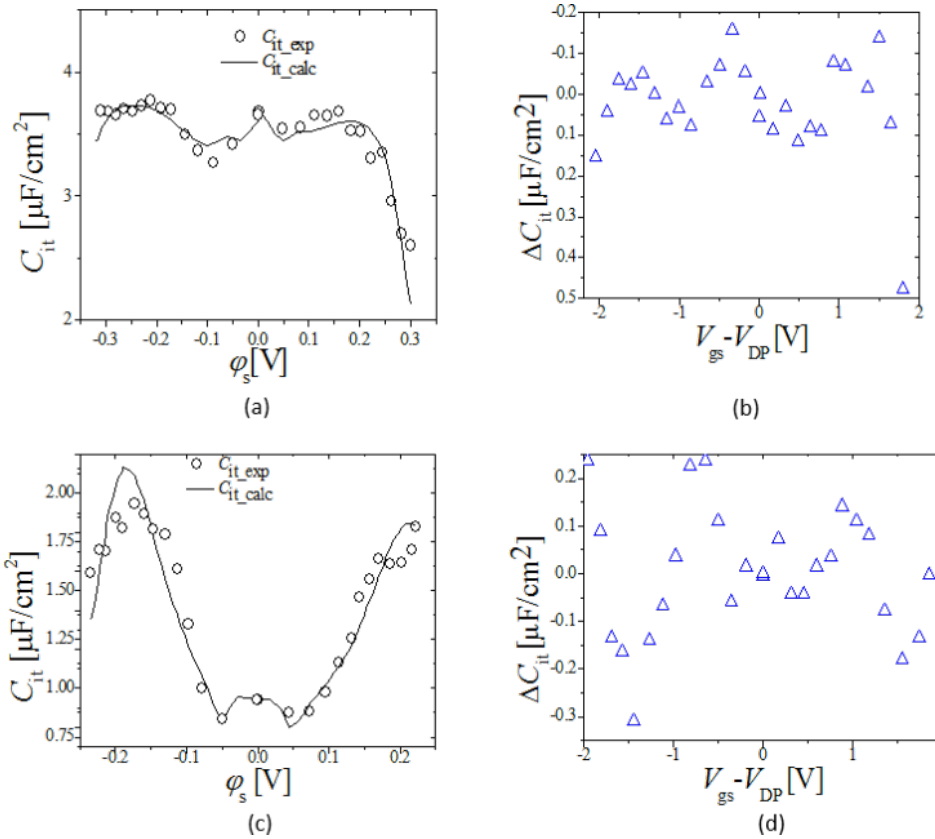

Figure 7: (a) and (c). C_{it} for Device 1 and 2 respectively, symbols: C_{it_exp} from Equation 6 as a function of φ_{s_exp}, line: C_{it_calc} calculated from Equation 8–11 as a function of φ_{s_calc}. (b) and (d) show the difference between C_{it_exp} and C_{it_calc} as a function of V_{gs} for Device 1, and 2 respectively.

Finally, C_{tot_exp} is compared with C_{tot_calc} calculated using C_{q_calc} from Equation 1, and C_{it_calc} obtained above in Equation 2, this is shown in Figure 8a and 8b for Device 1 and 2 respectively; C_{tot_exp} (symbols) is in excellent agreement with C_{tot_calc} (solid line). All calculated parameters dependent on D_{it} states, i.e., Q_{it_calc}, C_{it_calc}, φ_{s_calc} and device C_{tot_calc} are in

excellent agreement with the respective extracted experimental parameters, thereby validating the extracted D_{it} distribution.

It must be mentioned part of this work is based on our earlier work on MoS_2 transistor [14] as briefly mentioned earlier. However, in that work the interface trap density of MoS_2 tran-
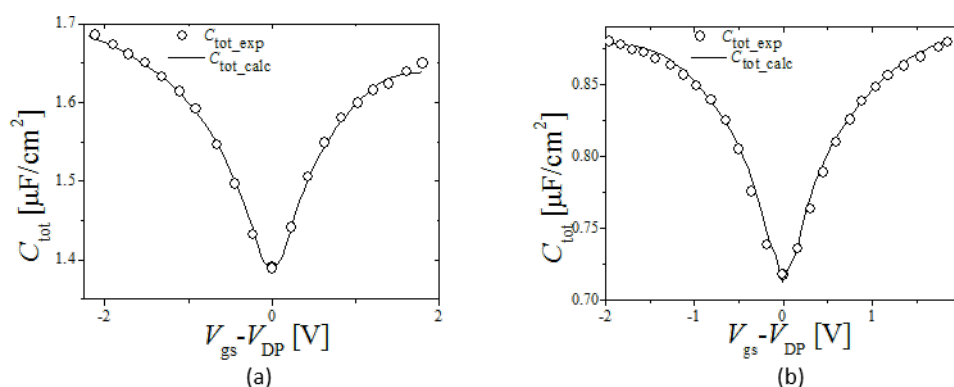
Figure 8: (a) and (b) C_{tot} for Device 1 [7] and 2 [12] respectively, symbols: C_{tot_exp} as a function of V_{gs}, lines: C_{tot_calc} from Equation 2 as a function of V_{gs}.

sistor was extrated by simply fitting the Q_{it} parameter in the device's drain current (I_{ds}) model to fit experimental device's I_{ds} with the calculated one from the model. Next, device's φ_s was calculated from the model equation. This φ_s was substituted in Equation 9–11 (also used in that work) to fit $E_{tA/D}$ and D_{it} values to match Q_{it} obtained earlier by fitting device's I_{ds}. This D_{it} distribution extraction procedure is the same in both works. However, in this work, instead of fitting Q_{it} in a drain current expression, a thorough analytical framework has been developed, based on fundamental MOGFET device physics, to extract important experimental parameters including Q_{it}, C_{it} and φ_s data from experimental $C_{tot}-V_{gs}$ data as highlighted in the section "Experimental φ_s, C_{it}, and Q_{it} extraction". Using these experimental parameters as a reference and the framework developed earlier [14,15] an analytical framework was presented to extract the interface trap distribution of MOGFET devices.

To date, to the best of our knowledge this is the only such work in the field. No thorough quantitative, experimental data yet exists on interface trap distribution of graphene transistors. In light of this, this work will be a useful addition to graphene-transistor compact modeling literature.

Conclusion

In summary, a simple analytic method was introduced to extract the interface trap distribution of MOGFET devices using device's $C_{tot}-V_{gs}$ data. The model makes use of the basic set of equations used to define device physics of MOGFET devices. Using the procedure mentioned above, interface trap densities of two reference experimental devices were extracted. Device parameters dependent on the extracted interface distribution including the calculated surface potential, interface trap charge, interface trap capacitance and total capacitance matched very well with the respective extracted experimental device parame-

ters. The model enables calculation of device surface potential with the adverse effect of trap charge on device surface potential included. This capability could further be explored in surface potential based MOGFET I_{ds} models to help predict MOGFET $I_{ds}-V_{gs}$ performance more accurately by including the effect of interface trap charge on device surface potential.

Acknowledgements

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