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# Metrology and technology computer aided design for the sub-10 nm technology node

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BEILSTEIN JOURNAL OF NANOTECHNOLOGY

# Absence of free carriers in silicon nanocrystals grown from phosphorus- and boron-doped silicon-rich oxide and oxynitride

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Full Research Paper

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## Abstract

Phosphorus- and boron-doped silicon nanocrystals (Si NCs) embedded in silicon oxide matrix can be fabricated by plasma-enhanced chemical vapour deposition (PECVD). Conventionally, $SiH_4$ and $N_2O$ are used as precursor gasses, which inevitably leads to the incorporation of ≈10 atom % nitrogen, rendering the matrix a silicon oxynitride. Alternatively, $SiH_4$ and $O_2$ can be used, which allows for completely N-free silicon oxide. In this work, we investigate the properties of B- and P-incorporating Si NCs embedded in pure silicon oxide compared to silicon oxynitride by atom probe tomography (APT), low-temperature photoluminescence (PL), transient transmission (TT), and current–voltage ($I$–$V$) measurements. The results clearly show that no free carriers, neither from P- nor from B-doping, exist in the Si NCs, although in some configurations charge carriers can be generated by electric field ionization. The absence of free carriers in Si NCs ≤5 nm in diameter despite the presence of P- or B-atoms has severe implications for future applications of conventional impurity doping of Si in sub-10 nm technology nodes.

## Introduction

The conductivity type and free carrier concentration of a semiconductor can be controlled via doping. Conventional impurity doping requires the incorporation of a suitable foreign atom on a lattice site and its ionization by thermal energy. Therefore, the energetic position of a dopant in the bandgap has to be close to the respective band edges. For Si, typical dopant ionization energies are in the range of ≈50 meV. If the size of the Si crystal approaches the exciton Bohr-radius, strong quantum confinement sets in and the valence- and conduction band ground state energies shift to lower and higher energies, respectively. As a consequence, the dopant ionization energies increase, which decreases exponentially the free carrier density [1]. If a doped Si-nanovolume is embedded in a matrix of lower permittivity (e.g., a dielectric), the dopant charge is not fully screened in the silicon and a Coulomb interaction with its image charge in the dielectric occurs. Irrespective of quantum confinement, this so-called dielectric confinement increased the dopant ionization energy even further [2]. At the nanoscale, the incorporation of an impurity on a lattice site is also subject to an increased formation energy as compared to the bulk, so that despite of thermal activation via, e.g., a high-temperature annealing process a significant fraction of potential dopants will remain on interstitial sites [3]. The decreasing number of Si–Si bonds per Si NC atom is a crucial point for the increase of dopant formation energies [4]. These factors impede efficient impurity doping of Si nanovolumes and complicate applications of Si NCs in devices based on p–n-junctions such as solar cells or light emitting devices [5,6]. Furthermore, semiconductor device fabrication technology nodes target the sub-10 nm scale in the near future, i.e., length scales where the effects described above will appear.

Si NCs of a few nanometres in diameter (i.e., quantum dots) represent a good model system to study doping at the nanoscale. They can be fabricated by various methods [7-9] and doped either during growth [7] or post-growth [10]. A recent review provides a broad overview of all available techniques and approaches [11]. Here, we focus on the Si NC growth via phase separation of PECVD-deposited, P- or B-doped silicon-rich oxide thin films via annealing at high temperatures. Additionally, we focus on comparatively lowly doped samples (on the order of 0.1–1 atom %) to study the classical electronic doping of Si NCs. In contrast, dopant concentrations up to 60% (also referred to as hyperdoping) were shown to induce localized surface plasmon resonances and metal-like free carrier densities [12-15]. The standard PECVD precursor gasses for silicon oxide are $SiH_4$ and $N_2O$. Since Si-rich oxides have to be grown in O-depletion, some of the N-radicals present in the plasma react with the Si and are subsequently incorporated in the film. The resulting material is inevitably a Si-rich oxynitride (SRON) with in our case ≈10 atom % N [16]. Considering some safety issues, the oxidizing PECVD precursor gas can be replaced by $O_2$, which allows for N-free Si-rich oxides (SRO) [17]. In both cases, small amounts of $PH_3$ or $B_2H_6$ can be added during deposition to achieve P- or B-doped SRON or SRO, respectively.

In this study, we investigate the structural, optical and electrical properties of P- and B-incorporating Si NCs in both embedding dielectrics. We will show that, despite some minor differences in the four different sample configurations, no free carriers associated to a doping behaviour of P or B are observed.

## Experimental

Superlattices of $SiO_2$ and SRO, or respectively, SRON were deposited on Si and quartz glass substrates by PECVD using processes described in [16,17]. Small amounts of 1% $PH_3$/Ar, or respectively, 10% $B_2H_6/SiH_4$ were added to the Si-rich layers (both SRO and SRON) whereas in all cases the $SiO_2$ barrier layers remained undoped. All samples were annealed for 1 h in ultra-pure $N_2$ in a quartz tube furnace at 1100 °C (SRO) and 1150 °C (SRON). The thicknesses of the Si-rich oxide layers determine the mean size of the Si NCs to be of approximately the size of the initial layer thickness. Samples dedicated to luminescence and electrical measurements were post-annealed in the same furnace in pure $H_2$ gas at 450 °C for 1 h to enable the passivation of dangling bond defects [18]. For electrical measurements, MOS capacitors were processed by thermal evaporation of Al-contacts. Molecular $Cs^+$ secondary ion mass spectrometry ($MCs^+$-SIMS [19]; Cameca IMS-4f) with 3 keV $Cs^+$ (for SRO:P/B) and 5.5 keV (for SRON:P/B) $Cs^+$ was used to quantify sample composition including the P- or B-concentration by means of a calibrated standard. APT was measured with a LEAP™ 4000X Si (Cameca) with a pulsed UV laser (355 nm, 100 pJ, 250 kHz), a cooled specimen holder (≈40 K) and a chamber pressure of $10^{-12}$–$10^{-11}$ Torr. The atom detection efficiency is 57%. For data reconstruction IVAS™ software (version 3.6.6) was used. APT specimen (needle-shaped tips attached onto the apex of a Mo support grid) were structured using an Auriga (Zeiss) focused ion beam scanning electron microscope. PL was measured using a $LN_2$-cooled CCD camera attached to a single grating monochromator with excitation of a HeCd laser (325 nm line). Low-temperature PL spectra were measured from 5 to 300 K using a single-window continuous-flow liquid-He cryostat. TT-dynamics were measured in a standard pump and probe configuration by a laser system with 100 fs pulse length and 1 kHz repetition rate (Tsunami, Spitfire, Newport). The fundamental 800 nm output was partly used as a probe and partly frequency doubled to 400 nm and used as a pump. The measurements were done at

room temperature. *I–V* and *I–t* was measured under accumulation bias, in dark and at room temperature, with an Agilent B1500A semiconductor device analyser and a Cascade M150 Prober in a shielded dark box.

# Results and Discussion

## Dopant concentration and -incorporation

At first, we determine the P-concentration as function of $PH_3$-flux for SRO and SRON via $MCs^+$-SIMS measurements. For this task, special samples were fabricated consisting of several 50 nm-thick SRO:P and SRON:P layers with different $PH_3$-fluxes, separated by $SiO_2$ spacing layers (20 nm and 10 nm thickness, respectively). The SIMS depth profiles for as-deposited SRO:P and SRON:P are shown in Figure S1a and Figure S1b of Supporting Information File 1. It turns out that the P-concentration in SRO:P can be adjusted by the available $PH_3$-flux from 0.59–4.61 atom %, while for SRON:P the range is limited to 0.18–0.71 atom %. In Figure S1c and Figure S1d of Supporting Information File 1 the SIMS depth profiles for similarly configured SRO:B and SRON:B layers are shown. Here, the B-concentration is controlled by the $B_2H_6$-flux in the range from 0.13–1.32 atom % for SRO:B and 0.02–0.14 atom % for SRON:B. When plotting the P- and B-concentrations in the Si-rich oxides as function of the flux ratio of $PH_3$ and $SiH_4$ or $B_2H_6$ and $SiH_4$, respectively, a quasi-linear dependence is found; see Figure 1. Generally, the dopant concentrations in SRON are lower than in SRO, which is caused by the very different precursor gas flows used in the SRON [16] and SRO [17] recipes. Nevertheless, for both dopants there is a concentration overlap region (indicated by grey boxes in Figure 1) for P in the range of 0.6 ± 0.1 atom % and for B in the range of 0.13 ± 0.02 atom %. Any direct comparison between doped SRO and SRON samples should hence be made in that overlap region to allow for equal nominal dopant concentrations. While the dopant-precursor flows are similar for each Si-rich oxide type, the average concentration of dopants is a factor of ≈5 lower for B than P, although the same amount of $B_2H_6$ gas contains twice the number of dopant atoms compared to $PH_3$. As a consequence, the incorporation efficiency of B in Si-rich oxides is approximately one order of magnitude lower than that of P.

Since SIMS cannot reveal the distribution of the dopants in the heterogeneous sample system of Si NCs and $SiO_2$ after annealing, atom probe tomography (APT) is used. APT was demonstrated to be a powerful method to reveal structural details of impurity elements in Si NCs [20,21]. In order to determine the incorporation of P-atoms into Si NCs, APT was measured for samples with SRO:P-0.59 atom % (for an image of a typical 3D-reconstruction see Figure 2a) and SRON:P-0.71 atom %. The mass spectra can be found in Figure S2 of

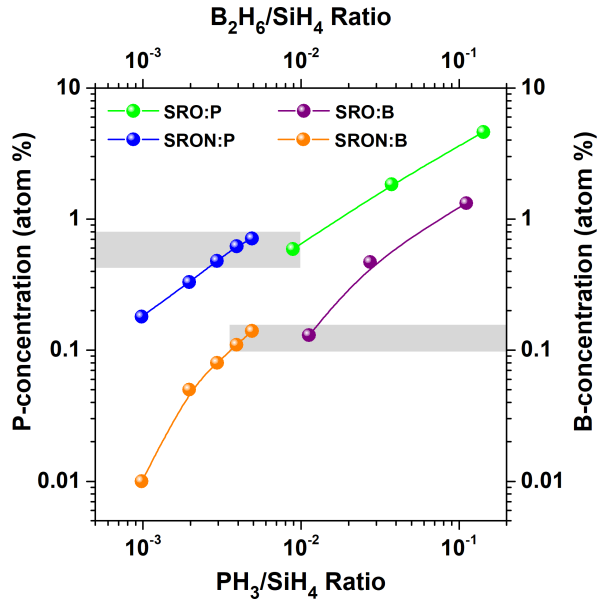



**Figure 1:** P- and B-concentrations as measured by $MCs^+$-SIMS as function of $PH_3$ to $SiH_4$ gas flow ratio, or respectively, as function of $B_2H_6$ to $SiH_4$ gas flow ratio for both SRO and SRON PECVD-recipes. The lines are just a guide to the eye to indicate the nearly linear dependences. The grey boxes indicate the concentration overlap regions for P- and B-doped SRO and SRON materials, respectively.

Supporting Information File 1. For reference and to exclude critical mass spectra peak overlaps of, e.g., $^{31}P^+$, $^{30}Si^{16}O_2^{2+}$, and $^{30}Si^1H^+$ an additional P-free sample was measured and no other signals influencing the ascription to P were found. Furthermore, the signals at 14 Da (Dalton, i.e., the unified atomic mass unit) and 28 Da indicate a very small influence of N on the mass spectra, which is consistent with its rather high ionization energy. Signals of $^{14}N^{2+}$ at 7 Da and $^{14}N_3^+$ at 42 Da in the mass spectra are assigned to N-ion peaks but their contribution is too small to quantify the amount of N. The determination of P-ions in the mass spectra in this study was carried out without further data correction (e.g., for delayed evaporation events, so-called thermal tails). Still, the method to analyse the data of both SRON and SRO samples is the same, thus, P-concentrations are directly comparable to each other. In Figure 2b the proxigram analyses (proximity histograms) [22] of all detected NCs in the respective samples are shown. As selected in previous works, the Si NCs were created by 70 atom % Si iso-concentration surfaces [23]. A voxel size of 0.5 nm and a delocalization value of ($x$, $y$, $z$) = (1 nm, 1 nm, 1.5 nm) were used [24]. The bin size of the proxigram was set at 0.1 nm. Note that these parameters do not change the trend of the composition profiles of both samples. On first sight, no significant differences in the distribution of P-atoms in the NC-interior, at the $Si/SiO_2$ interface, and in the $SiO_2$ matrix are found. Especially the interior of the Si NCs and the near-interface region of the $SiO_2$ have almost identical P-concentrations of

≈0.5–0.7 atom %, while in the N-free $SiO_2$ matrix apparently less P is dissolved (≈0.2 atom %) compared to the oxynitride matrix (≈0.3 atom %). However, given the 20% (relative) higher initial P-concentration in SRON:P compared to SRO:P and a measurement uncertainty in the range of 0.1 atom %, this difference might be negligible. The overall P-distribution corresponds very well to previously observed trends for P in Si NCs [23-26]. We note that the ≈20% O-concentration in the NC-interior is an artefact from local magnification effects (LME) [27,28] which is generally observed in this material system [24-26,29,30]. Inevitably, this artefact also influences the exact values of the P-concentration, but since both samples are subject to the same LME the comparison discussed above is not influenced. Besides LME there are also other factors influencing the precision and resolution of APT such as inhomogeneous tip shape evolution during the measurement [31], delayed dissociation of molecules during the flight [32], and associated problems with the detection of neutral fragments [33]. Still, APT provides unique and very useful data inaccessible by any other method.

In Figure S3a of Supporting Information File 1 the NC-size distribution as derived from APT using iso-concentration surfaces of ≥70 atom % Si is plotted as well as the relative frequency of the number of P-atoms per NC. The number of P-atoms incorporated per NC and the P/Si-ratio, both as function of NC-volume, are shown in Figure S3b of Supporting Information File 1. While details of this data set are discussed in Supporting Information File 1, it can be readily concluded that the P-distribution and NC-incorporation is very similar for both SRO:P and SRON:P. Therefore, the presence of N in the oxynitride matrix has apparently no influence on the structural properties of P-doped NC-samples.

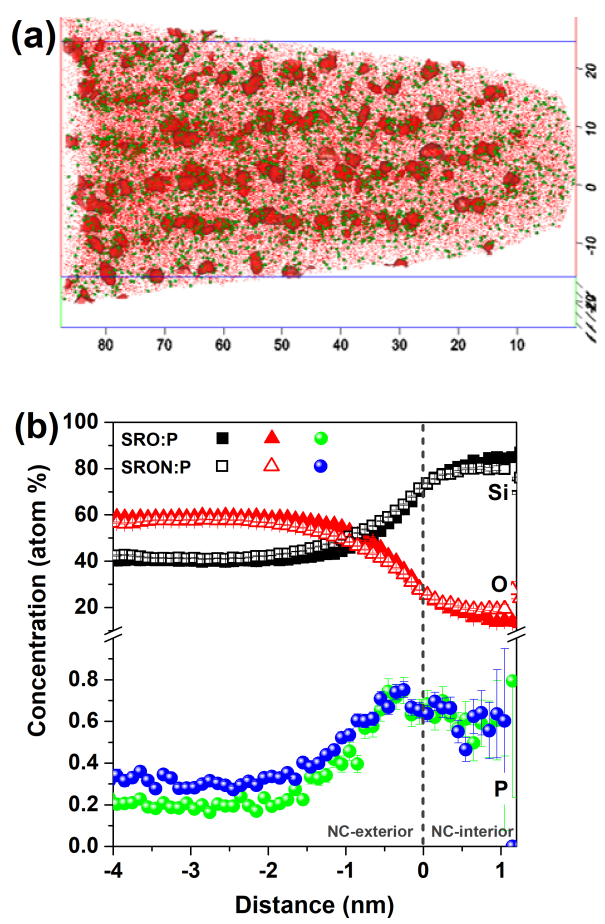



**Figure 2:** (a) Atom probe tomography reconstruction of P-doped Si nanocrystals (red iso-surfaces with ≥70 atom % Si) in N-free $SiO_2$ matrix (P-atoms: green; Si-atoms: red; all axes in nm). (b) Proxigram analysis of Si NCs grown from SRO:P (0.59 atom %) and SRON:P (0.71 atom %). The local P-concentrations are depicted in green for SRO:P and blue for SRON:P. Positive distances refer to the inner NC-volume, negative distances to the surrounding matrix.

The SRO:B material has already been APT-analysed in [30] with the result that B is generally less likely to be incorporated deep in the NC core but more near the inner surface (in agreement with former theoretical [34,35] and experimental [26] evidence). Due to the maximum B-concentration in SRON:B of only 0.14 atom %, a statistically meaningful APT-analysis cannot be achieved. However, the absence of any significant differences between SRON:P and SRO:P suggests that the nitrogen in the oxynitride matrix will not have a notable influence on the B-distribution when SRON:B and SRO:B are compared.

## Photoluminescence and transient transmission

Due to quantum confinement effects the ground state energy of Si NCs increases and the k-space overlap of electron and hole wave functions are significantly enhanced (Heisenberg's uncertainty principle). Therefore, excitons formed in Si NCs are subject to significantly higher radiative recombination probabilities, allowing the luminescence quantum yield to reach ≈30% [36,37], or even ≈60% for organically-capped NCs [38]. In the presence of a third charge carrier (a free electron from an ionized P-donor or a hole from an ionized B-acceptor) radiative recombination is very unlikely, since ultra-fast non-radiative Auger recombination will prevail [7]. On the other hand, the observation of PL quenching alone cannot prove the presence of free carriers since also dopant-induced defects can be involved [29,30,39-41]. In Figure 3a, the dependence of the PL spectra on the P-concentration in SRO:P and SRON:P is demonstrated. Here, all samples are $H_2$-passivated and hence only the PL-quenching effect of P-incorporation is visible, not the PL-enhancement often observed for low P-concentrations and associated to dangling bond passivation by P [42]. Up to the level of ≈0.6 atom % P the PL intensity drops by less than 40%

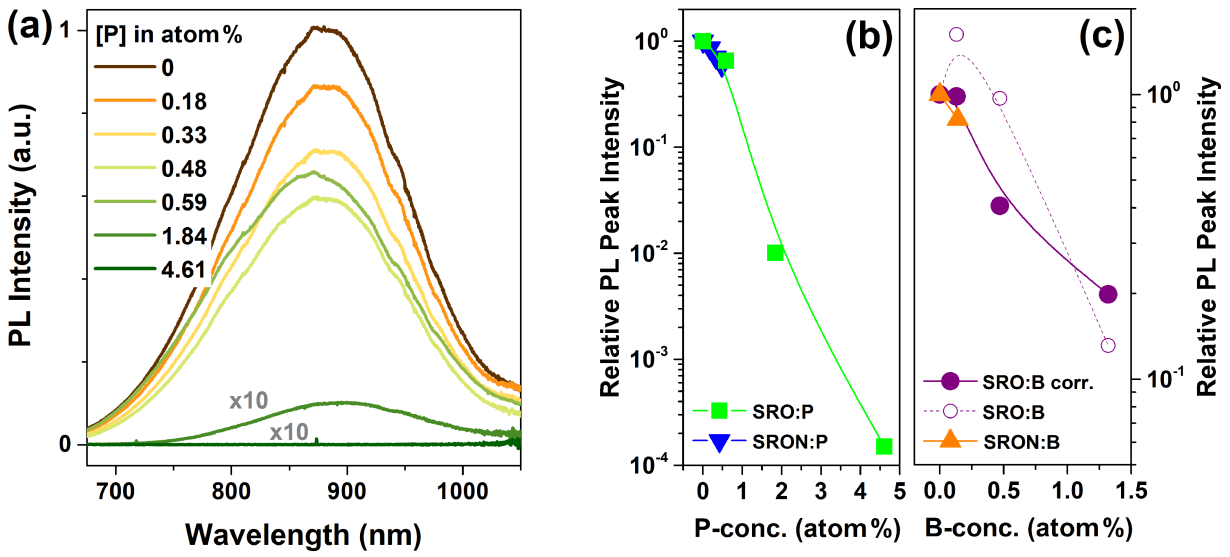



**Figure 3:** (a) Room temperature photoluminescence spectra of P-incorporating Si NCs in SRON (0–0.48 atom %) and SRO (0.59–4.61 atom %). The spectra of the two highest P-concentrations are multiplied by a factor of 10 for better visibility. (b) and (c) logarithmic PL peak intensity as function of P-concentration, or respectively B-concentration, in SRO and SRON, normalized to the respective dopant-free samples. For SRO:B-samples the PL-intensities are corrected for the excess-Si content (open purple circles show the raw data). Lines are just a guide to the eye. For both dopants it is obvious that significant PL-quenching requires P-/B-concentrations >1 atom %.

without any significant peak shift. According to the APT data shown above and in Supporting Information File 1 only the smallest NCs of each sample remain rather P-free and therefore potentially PL-active, which would implicate a strong PL blueshift, if Auger quenching by P-donors is considered. From Figure 3a and 3b, however, it is obvious that neither a spectral shift nor an efficient PL-quenching by P-incorporation takes place. In contrast, the PL remains very intense up to a P-concentration in SRO beyond >1 atom % P, i.e., vastly exceeding the solubility limit of P in Si. An almost complete suppression of PL occurs only for samples with 4.61 atom % P. Within the concept of PL-quenching by free-carriers induced by P-atoms in the Si NCs, it remains dubious why concentrations of several atom-percent should be required although APT detects in the majority of NCs already one or several P-atoms for samples with 0.6–0.7 atom % P. It appears more consistent with the available data that P-induced defects (e.g., from interstitial P in the Si NCs or $SiO_x$:P-related states at the surface) cause the PL quenching, as supported by density functional theory (DFT) calculations [29,41]. In that context, it is also likely that for samples with >1 atom % P the P-concentration peak found at the $Si/SiO_2$ interface (cf. Figure 2b) reaches a level where a highly enriched P-shell forms on the NC-surface that enables efficient formation of non-radiative defect states.

For boron, strong PL-quenching is also not observed before the B-concentrations exceed >1 atom %, as shown in Figure 3c, and the same argumentation holds true for B-induced defects with states in the fundamental gap of Si NCs, as determined by DFT [30]. The as-measured PL peak intensity of the SRO:B sample set (open purple circles) is unfortunately obscured by variations in the initial excess-Si content (cf. Figure S1c of Supporting Information File 1), which directly influences the NC-density in those samples. Hence, the data set is corrected by the excess-Si content as measured by $MCs^+$-SIMS (filled purple circles in Figure 3c; for details see caption of Figure S1 of Supporting Information File 1).

We note that the overall PL-quenching behaviour of Si NCs in doped SRO and SRON is similar. Hence, the presence of nitrogen in the matrix does not have a major impact on the formation of B- or P-induced centres that quench the PL.

Electronic doping, i.e., the generation of free carriers from dopants on substitutional lattice sites, requires thermal ionization, typically provided by the thermal energy at room temperature. Ignoring all the evidence of a defect-related PL-quenching of Si NCs containing P- or B-atoms, we would anticipate from low-temperature PL measurements of successfully, electronically doped Si NCs: (i) an increase in the PL-intensity as soon as free carriers are frozen out, accompanied by (ii) a spectral redshift due to the circumstance that within the NC-size ensemble the largest NCs are more easily doped than the smaller NCs, and (iii) significant differences in the PL peak behaviour when compared to undoped reference samples. In Figure 4, the T-dependent PL-peak analyses of spectra measured at very low exci-

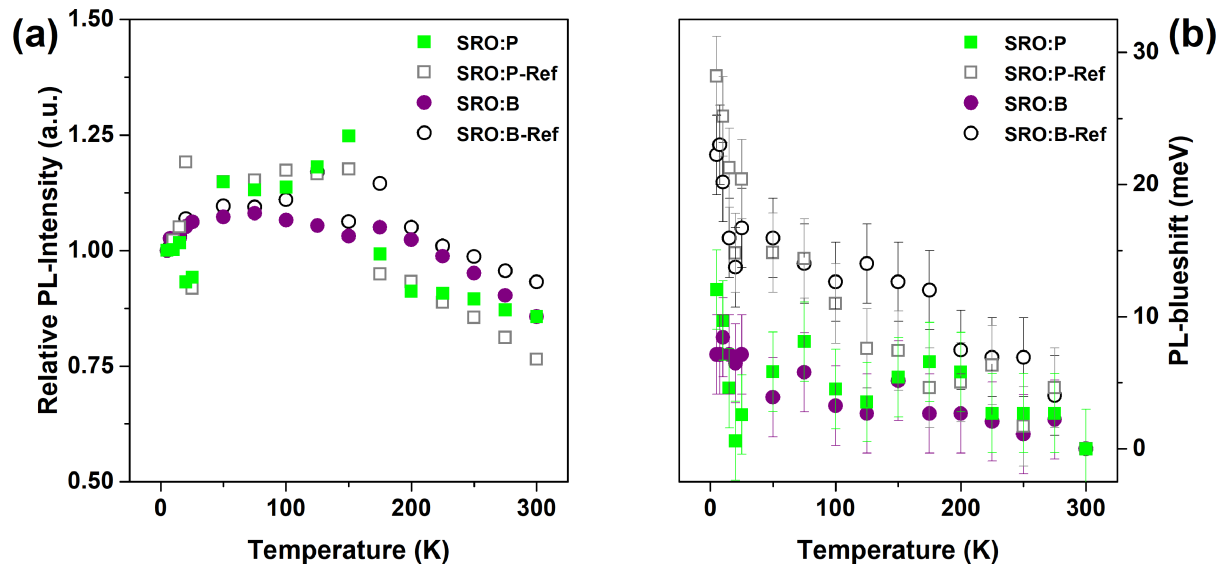



**Figure 4:** Low-temperature PL data of samples with 5 nm SRO and 0.59 atom % P (SRO:P), 0.47 atom % B (SRO:B) and their respective intrinsic references (SRO:P-Ref, SRO:B-Ref). (a) Relative PL-intensities with respect to the measured value at 5 K of each sample, i.e., the lowest temperature where all potential dopant-induced carriers are completely frozen out. There is hardly any difference visible in the PL-intensity over temperature between doped and undoped samples. (b) PL peak shift with reference to the peak at 300 K, i.e., where ionized donors and acceptors would quench predominantly the largest NCs in each sample. A slight PL-blueshift is observed, not a redshift as expected from NC-doping.

tation fluxes of ≈0.4 mW/cm$^2$ (to prevent over-excitation artefacts [43]) are presented. The spectra themselves can be found in Figure S4 of Supporting Information File 1. Figure 4a shows the relative PL-intensity as function of sample temperature ($T$) with respect to the intensity at 5 K, where all free carriers from potential dopants would be completely frozen out. The intensity trends follow roughly the low-excitation measurements shown in [44]. For approx. $T > 150$ K the intensity drops below unity due to the thermal activation of non-radiative recombination channels [36,44]. The relative PL-intensities of all samples with respect to their 5 K values end up in the same range of values at room temperature. Hence, a freeze-out effect of dopant-induced free carriers that quench the PL is not observed in accordance with dopant-induced defect states deep within the fundamental gap of the NCs.

Figure 4b plots the PL peak shift with reference to 300 K, i.e., where a maximum of dopant-induced free carriers would quench the PL, which would preferentially affect the larger NCs with least confinement energy. Instead of a PL redshift expected for doped NCs with decreasing $T$, we observe a small blueshift related to the thermal contraction of the lattice and reduced electron–phonon interaction, which typically saturates around 100–200 K for lowly excited samples [43]. To add, the blueshift of the reference samples is slightly more pronounced for $T < 150$ K than that of the doped samples. The increase for $T \leq 25$ K is most likely an artefact from overexcitation [43] despite the very low laser intensity. The reason for using two nominally identical reference samples (both are undoped SRO) in PL is due to the different number of NC-layers in the superlattice (10 for SRO:P and 20 for SRO:B). Any differences between the reference samples might therefore be interpreted as the scattering amplitude between different samples.

In Figure 5 we report the transient transmission dynamics of samples with 4.5 nm Si NCs made of (a) SRON:P with 0.71 atom % P and (b) SRO:B with 1.32 atom % B, i.e., samples with substantial incorporation of dopant atoms and significant PL quenching. For this measurement the excitation pump pulse wavelength was 400 nm (efficiently absorbed by the NCs) and the probe pulse wavelength was 800 nm, which is hardly absorbed by the NCs. However, if free carriers are present in the NCs, whether from optical excitation or from doping, the probe light is absorbed. The transmission of the sample at the probe wavelength in the unexcited state is measured as $T_0$ and the transmission as function of delay time between pump and probe (in steps of ≈100 fs) is plotted as

$$\frac{T - T_0}{T_0}.$$

The pump flux is chosen to generate only a few excitons per NC [45]. Specifically, 2.3 mJ/cm$^2$ (SRON) and 3.4 mJ/cm$^2$ (SRO) were used, which correspond to the excitation regime with normal Auger recombination of excitons, excluding bimolecular recombination [46]. If an additional free carrier (electron

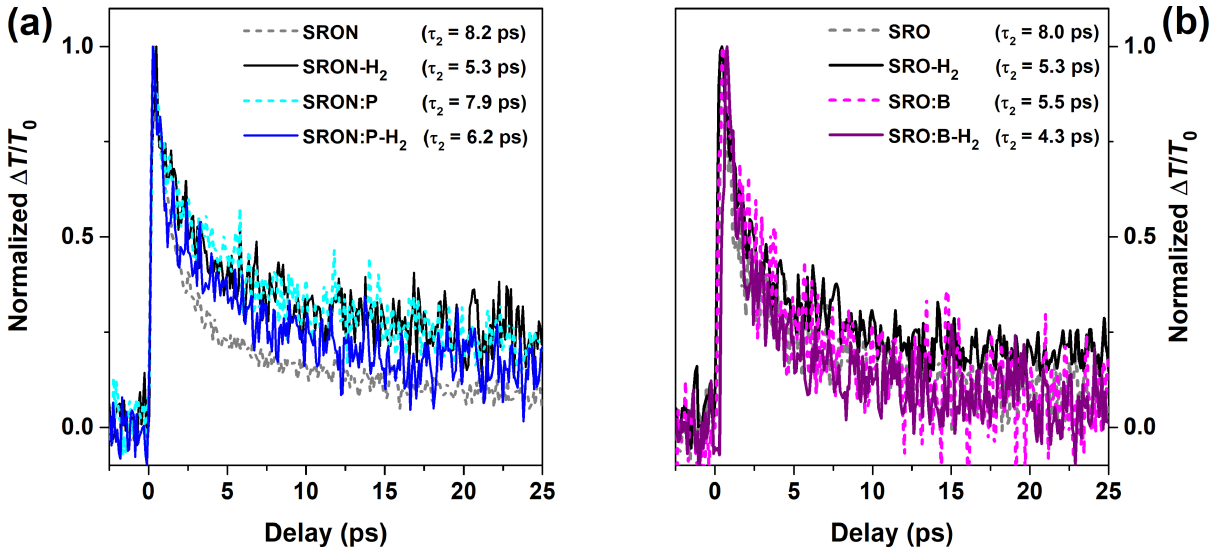



**Figure 5:** Transient transmission (TT) dynamics from pump-probe measurements at room temperature of ≈4.5 nm Si NCs from (a) SRON:P and P-free SRON and (b) SRO:B and respective B-free SRO. All samples are measured before and after $H_2$-passivation. The curves are normalized for better comparability of the decay dynamics (although no significant or even doping-related differences exist in the initial signal intensity of the samples). The time constants of the component $\tau_2$ of the two-exponential fits (not shown for clarity) are given in the figure. The presence of P- or B-atoms in the NCs does not increase the speed of carrier recombination, as would be expected from the presence of dopant-induced free carriers.

from P-donor or hole from B-acceptor) would be present in a Si NC, the generated exciton(s) could efficiently and quickly recombine with the unpaired charge carrier via an Auger process. This would substantially accelerate the reduction of the total carrier density and a doped sample would become transparent in shorter time as compared to an intrinsic sample. It is obvious from Figure 5a and 5b that neither for SRON:P nor for SRO:B accelerated TT-dynamics exist. When fitting the curves, best results are obtained for a two-exponential fit

$$\frac{\Delta T}{T_0} \sim e^{-t/\tau_1} + e^{-t/\tau_2},$$

where the fast component $\tau_1 \approx 0.5 \ldots 1.5$ ps for all samples is attributed to ultrafast carrier trapping and thermalization events. The long component $\tau_2$ is associated with the actual Auger recombination of excitons and ranges from 5 to 8 ps without differences between doped or undoped samples. We conclude that no measurable initial carrier densities exist at room temperatures in P- or B-doped Si NCs in silicon oxide matrix.

The TT-results are presented for both $H_2$-passivated and unpassivated states without distinctive differences, but one remark concerning the interaction of Si-doping and hydrogen shall be made: While P in the Si NC system is known to passivate dangling bonds (DBs) at the $Si/SiO_2$ interface [7,42] similar to a post-annealing in $H_2$, hydrogen treatments have also been shown to deactivate P-donors and B-acceptors in heavily doped Si nanowires [47] and in the bulk [48-50]. However, this type of dopant passivation solely relies on very reactive atomic hydrogen (rather than molecular $H_2$ gas) and requires much lower temperatures of 100–150 °C to be efficient. When considering $H_2$ as used in our work, the effective (endothermic) dissociation enthalpy of the reactions 2 P-DB + $H_2$ → 2 P-H and 2 Si-DB + $H_2$ → 2 Si-H yield ca. 0.05 eV and ca. 0.09 eV per DB passivation, respectively [51]. This finding renders the P–H bond breakage to occur at significantly lower temperatures as used at $H_2$ anneals to passivate Si-DBs (450–500 °C).

Such a H-passivation mechanism of dopants requires their substitutional incorporation, which occurs apparently only in very small fractions for dopants in Si NCs (see section Electrical properties below). Therefore, neither from experimental evidence nor from fundamental considerations, it can be argued that the doping effect of P or B in Si NCs is obscured by $H_2$-passivation. In contrast, the passivation of DB-defects at the $Si/SiO_2$ interface often improves the interpretability of the measured data.

## Electrical properties

If free charge carriers would be present in the Si NCs, or if they are generated via ionization by an external electrical field, it is possible to detect their presence by *I–V* measurements on MOS-capacitors with additional injection barriers [52,53]. Respective samples (injection-blocking MOS-capacitors) were fabricated with 10 nm-thick $SiO_2$ buffer and capping layers to prevent low-field injection of carriers from either substrate or gate, so that only transient displacement currents are measured. The cur-

rent density over electric field (*J*–*E*) curves of B- or P-incorporating SRO and SRON samples, together with dopant-free reference samples, are depicted in Figure 6. None of the reference samples (dashed lines) shows a current peak in the low E-field regime, which excludes significant contributions to the displacement current by undoped Si NCs or their host matrices (pure oxide vs oxynitride). The *J*-curves of the P-incorporating NCs show a broad peak at ≈0.5 MV/cm for SRO:P and a sharper peak at ≈0.3 MV/cm for SRON:P. The peak character for SRO:P is less clearly expressed. Whereas the rising shoulders of both *J*-peaks are quite similar, only for the SRON:P sample the current density decreases behind the peak with a comparable slope but remains on a plateau for SRO:P. The origin of the *J*-signal is the ionization of substitutional P-atoms in Si NCs and the subsequent accumulation of the "free" charge carriers under the gate blocking oxide (cf. [29] and [52] for details). Following the calculations therein, we can estimate the P-ionization energy of the *J*-peak (or respectively the beginning of the *J*-plateau) to ≈200 meV, in accordance with literature values on ionization energies of nano-sized Si [54,55]. For SRO:P the *J*-plateau indicates a broader distribution of P-ionization energies towards even larger values.

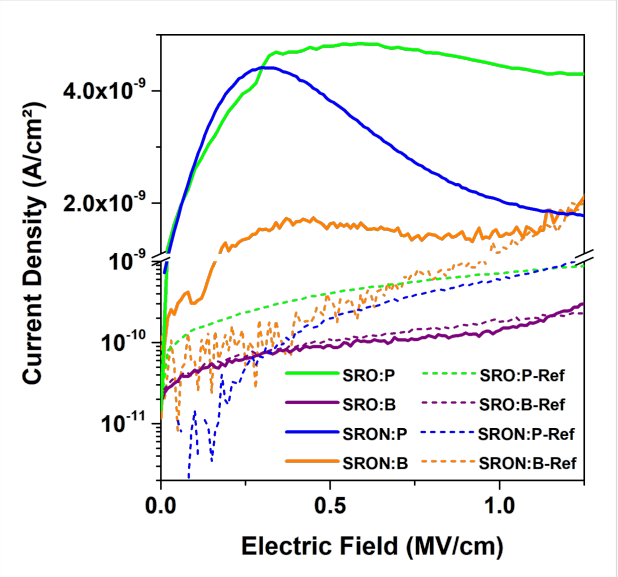



**Figure 6:** *J*–*E* data of injection-blocking MOS-capacitors with P- or B-incorporating Si NCs in SRO and SRON and their directly corresponding references (SRO:P with 0.59 atom %, SRON:P with 0.48 atom %, SRO:B with 1.32 atom %, SRON:B with 0.14 atom %).

The comparison between SRO:B and SRON:B is even more surprising: While Si NCs from SRO:B do not show a *J*-peak but rather identical *I*–*V* behaviour as the respective reference, the SRON:B sample shows a weak plateau-like peak at ≈0.4 MV/cm. It is emphasized that the *J*-peak is found in the maximum possible B-doped SRON sample, but not in the max-doped SRO:B sample, despite an almost one order of magnitude higher B-concentration in the latter. Hence, B-doped Si NCs may be field-ionized in SRON, in contrast to our previous report on SRO [30] and in accordance with [53]. The hole-tunnelling properties of the matrix seem to determine the visibility of this effect and oxynitride seems to allow for a better hole transport (maybe assisted by N-related states), while N-free pure oxide apparently camouflages the field-ionization of B in SRO:B. In the case of electrons from field-ionized P-donors the situation is less critical since the conduction band offset of Si NCs and $SiO_2$ is only about half that of the valence band offset [56].

Figure 7a shows *I*–*t*-transients of the injection-blocked MOS-capacitors (the inset depicts a schematic cross-section) measured at 0.2 MV/cm, i.e., at the onset of the *J*-peak/plateau (if present). As expected from the device geometry, all transient displacement currents reach the noise level at the minimum detectable limit (sub-pA range), which marks the end of the measurements. Whereas the fast drop of *J* of the reference samples within the first seconds of the measurement is attributed to dielectric relaxation, the P-doped Si NC samples clearly show mobile charge redistributions on a longer timescale. For the B-doped Si NCs the situation is less clear, since the noise level is reached earlier. A likely cause for this behaviour might be a lower density of redistributable charge. With the exception of SRO:B samples, there is also a 1–2 orders of magnitude higher *J*-level throughout a major part of the transient period between the doped samples and their respective references. By integrating the measured current over time, the corresponding total charge, generated by field ionization of dopants on Si-lattice sites in the NCs, can be estimated [52]. The free carrier densities of all samples at 0.2 MV/cm are shown in Figure 7b. Values of $(4 \pm 3) \times 10^{15}$ $cm^{-3}$ were obtained for the reference samples (grey open circles); we note that these values are strongly influenced by dielectric relaxation. From the doped samples (black filled circles) only SRO:B has a similar value (being slightly below its reference). All other doped NC-samples have free carrier concentrations in the $10^{16}$ $cm^{-3}$ range. In order to exclude a contribution to the free carrier values from the dielectric relaxation, we subtract the reference-values to obtain the effective free carrier density ($N_{F,eff}$, red spheres in Figure 7b). It is obvious that P dominates over B and SRON over SRO: Sample SRON:P has about twice the integral charge than SRO:P and SRON:B is an order of magnitude lower than SRON:P. In this context, point out that SRON:B has a B-concentration that is just 30% of the P-concentration in SRON:P. Although the initial dopant concentration in the Si-rich oxide is not the figure of merit but the substitutional incorporation in the NCs, these results still indicate that B-doping is less efficient than P-doping. This is underlined by

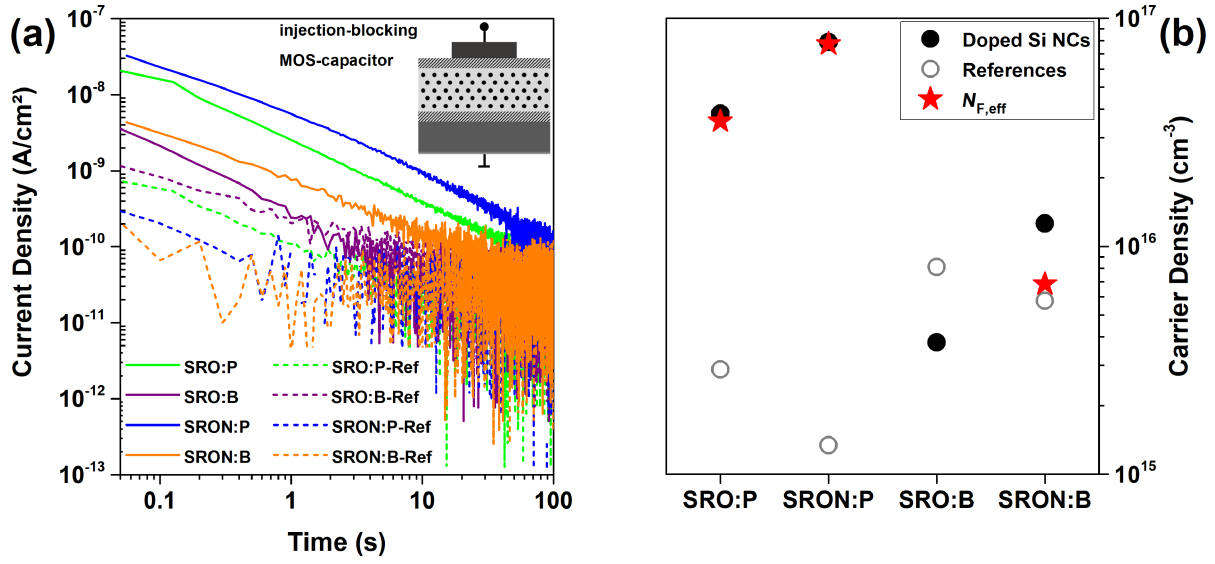



**Figure 7:** (a) *J–t* transients of the same MOS-capacitors as in the previous figure measured at *E* = 0.2 MV/cm. The inset shows a schematic cross-section of the device under test. (b) Free carrier density from field ionization of substitutional dopants derived from integrating transient current over time. For effective free carrier values ($N_{F,eff}$) the values of the dopant-free references values are subtracted from the values of the doped Si NC samples.

the electrical properties of the SRO:B samples, which do not even have a positive effective free carrier density. Here, the very small effective free carrier density of SRO:B is exceeded by the carrier density of SRO:B-Ref, which might originate from the slightly different NC-density caused by the B-dependent Si-content (cf. Figure S1, Supporting Information File 1). We note that for SRON:P a field ionization doping efficiency of ≈4% was derived by dividing $N_{F,eff}$ with the number of P-atoms in the NCs measured by APT [29], which allows to estimate for Si NCs from SRO:P a field ionization doping efficiency of ≈2%, whereas for SRON:B in absence of measurable APT results no efficiency can be estimated.

## Conclusion

Comparing oxynitride and N-free oxide as matrix for P- or B-incorporating Si NCs, no significant differences were observed structurally (SIMS, APT) or optically (PL, TT). Electrically (*I–V*, *I–t*) differences occur, which appear to be related to the insulating nature of the oxide matrix itself and the respective band offsets. For both dopants a slight room-temperature PL quenching is observed, becoming strong only for dopant concentrations beyond 1 atom %. This circumstance together with the absence of the spectral behaviour expected for doped NCs indicates that dopant-induced defects are the origin of PL quenching, in accordance with theoretical DFT predictions. Low-temperature PL spectroscopy and transient transmission measurements show no indications for dopant-induced free carriers in Si NCs. Electrical measurements on MOS-capacitors with additional injection blocking layers prove that E-fields in the range of 0.3–0.5 MV/cm are required to ionize the small fraction of lattice-incorporated dopants and to generate charge carriers. It was shown that the higher resistivity of the N-free oxide as compared to oxynitride masks the field-induce charge carrier generation from B-doped NCs. Comparing P-doped NCs in both matrices this effect was not found.

Summarizing the results reported here and previously [29,30,41,52] it turns out that P- and B-dopants in oxide-embedded Si NCs remain predominantly on interstitial lattice sites where they cannot be ionized by thermal energy at room-temperature, in agreement with the nanoscale-effects of self-purification, quantum- and dielectric confinement. This results in diminutive doping efficiencies [57]. We note that broader NC size distributions with tails towards the ≈10 nm range [58] or percolated nano-Si networks [53] are not subject to the same strong confinement conditions, so that measurable free carrier densities are likely.

The fundamental inability of efficient conventional impurity doping at the bottom end of the nanoscale requires different doping approaches that either relocate the dopants in the surrounding matrix (e.g., Si modulation doping by $SiO_2$:Al) [59] or do not require impurities at all (e.g., electrically reconfigurable nanowire-FETs [60] or *p*/*n*-behaviour induced by energy offsets created by locally $Si_3N_4$ and $SiO_2$ embedded Si-nanowires [61]).

## Supporting Information

### Supporting Information File 1

Additional figures.
[https://www.beilstein-journals.org/bjnano/content/supplementary/2190-4286-9-141-S1.pdf]

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# The role of the Ge mole fraction in improving the performance of a nanoscale junctionless tunneling FET: concept and scaling capability

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Full Research Paper

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## Abstract

In this paper, a new nanoscale double-gate junctionless tunneling field-effect transistor (DG-JL TFET) based on a $Si_{1-x}Ge_x$/Si/Ge heterojunction (HJ) structure is proposed to achieve an improved electrical performance. The effect of introducing the $Si_{1-x}Ge_x$ material at the source side on improving the subthreshold behavior of the DG-JL TFET and on suppressing ambipolar conduction is investigated. Moreover, the impact of the Ge mole fraction in the proposed $Si_{1-x}Ge_x$ source region on the electrical figures of merit (*FoMs*) of the transistor, including the swing factor and the $I_{ON}/I_{OFF}$ ratio is analyzed. It is found that the optimized design with 60 atom % of Ge offers improved switching behavior and enhanced derived current capability at the nanoscale level, with a swing factor of 42 mV/dec and an $I_{ON}/I_{OFF}$ ratio of 115 dB. Further, the scaling capability of the proposed $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET structure is investigated and compared to that of a conventional Ge-DG-JL TFET design, where the optimized design exhibits an improved switching behavior at the nanoscale level. These results make the optimized device suitable for designing digital circuit for high-performance nanoelectronic applications.

## Introduction

In the last years, the continuous miniaturization of nanoscale transistors induces new challenges including short-channel effects (SCEs) and high power consumption, which prevent incorporating conventional metal-oxide semiconductor field-effect transistors (MOSFETs) and their complements in nanoelectronic circuit designs [1-4]. In this context, small swing-switch devices such as double-gate tunneling field-effect transistors (DG TFETs) are gaining attention because of their good subthreshold characteristics, high scalability and low OFF-current [5-8]. The main idea behind this innovative device is the use of a gated p-i-n diode, the working mechanism of which is based on a quantum band-to-band tunneling effect. This makes

it more immune against the undesired SCEs and enables a better scaling capability. Despite such attractive properties, DG TFETs still suffer from other issues mainly related to the relatively low ON-state current and the severe ambipolar conduction, which make it extremely challenging for designing high-performance digital nanocircuits [7-9]. Consequently, intensive efforts have been paid to address these limitations by proposing new designs based on heterostructures, gate engineering and high-*k* dielectrics [9-12]. Nanoscale DG TFETs are believed to face an upward amendment to meet the difficulty of decreasing the huge thermal budget required for the formation of the gated p-i-n diode structure. Moreover, in spite of the actual mature experimental techniques, realizing metallurgical junctions in sub-32 nm nodes is considered extremely difficult [13-15]. For this purpose, the junctionless (JL) design is considered the best approach to avoid the above outlined experimental limitations and achieve significant improvements regarding the transistor manufacturing cost [14-17]. The JL technology is considered to be cost-effective and allows avoiding the high thermal budget [15-17]. The concept of a gated source is used for the JL technology in order to ensure the band-to-band tunneling effect, while materials with high work function are required to generate the tunnel current. In other words, the channel is assumed to be a uniformly and highly doped *n*-type material, and in order to ensure the band-to-band tunneling effect, the source is supported with a control gate to make the device behave like a conventional p-i-n-based TFET [18]. However, the most pronounced drawbacks associated with the DG TFETs design also persist in the JL structure, namely the low ON-state current, the high leakage current and parasitic ambipolar conduction, which can eventually prevent the application in high-performance nanoelectronic circuits. The DG-JL TFET design can pave the way to reduce the fabrication cost, but it exhibits degraded electrical FoMs. Several recently published works are focused on improving the multi-gate JL TFET by suggesting design improvements such as gate underlap and overlap, introducing III–V materials and source/drain engineering [19-24]. Additional approaches are in fact required in order to push the limits of the DG-JL TFET performance and achieve energy-efficient and scalable transistors. To the best of our knowledge, no design approach based on $Si_{1-x}Ge_x$/Si/Ge heterochannels with optimized Ge content was proposed to improve the electrical performance and to suppress the parasitic ambipolar conduction in DG-JL TFETs. We present in this paper, a new DG-HJ-JL TFET design to achieve improved electrical FoMs and reduced fabrication cost. An exhaustive numerical study of the electrical behavior of the proposed device at the nanoscale level is performed using the ATLAS 2-D simulation software [25]. Further, the impact of the Ge content on the electrical performance of the transistor is investigated. It is found that the proposed design offers between improved derived current capability and reduced ambipolar conduction compared to a conventional DG Ge-JL-TFET design. In order to consolidate our investigation, the scaling capability of the proposed design is investigated and compared to that of the conventional counterpart, where the proposed structure demonstrates a superior switching behavior. This makes the optimized structure a potential alternative for providing energy-efficient transistors with suppressed ambipolar conduction for designing high-performance nanoelectronic circuits at low manufacturing cost.

## Numerical Simulations

Figure 1 describes schematically the investigated DG-HJ-JL TFET structure. The cornerstone of the proposed design is the assumption of a uniformly and highly doped heterochannel ($Si_{1-x}Ge_x$/Si/Ge), which can be indicated by $n^+/n^+/n^+$. In addition, the proposed design is suggested with a $HfO_2$ gate dielectric in order to ensure a good electrostatic control of the channel, with $t_{ox}$ representing its thickness. Moreover, the material of the gated source is assumed to have a high work function value of 5.6 eV in order to guarantee the tunnel effect, while the work function of the channel gate is set equal to 4.3 eV. In Figure 1, $L$ is the channel length, $t_{ch}$ refers to the channel thickness, $N_d$ is the doping concentration of the channel, and $L_s$ and $L_d$ denote the extension lengths of source and drain, respectively.

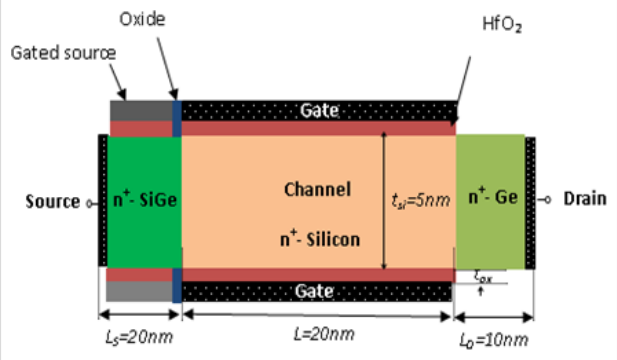



**Figure 1:** Schematic of the investigated DG-HJ-JL TFET with $N_d = 1{\cdot}10^{19}$ cm$^{-3}$ and $t_{ox}$ = 3 nm.

The accurate modeling of the nanoscale DG-HJ-JL TFET requires taking into account quantum-confinement effects, which lead to some modeling bottlenecks associated with the models of the carrier density gradient. Furthermore, since the investigated transistor is considered as a quantum mechanical device, complicated systems of equations resulted from the necessity of considering the band-to-band quantum tunneling effects. These nonlinear equations impose many mathematical difficulties, which complicate the analytical modeling of the nanoscale device performance. Numerical approaches are used

to deal with the above outlined problems. The ATLAS 2D device simulator using the S-PISCES module has emerged recently as a useful and realistic tool for numerically modeling the electrostatic behavior of transistors [25].

The electrostatic behavior of the investigated nanoscale ($Si_{1-x}Ge_x$/Si/Ge) DG-HJ-JL TFET including the tunnel effects is modeled using the nonlocal-BTBT command, which takes into account nonlocal band-to-band quantum tunneling [25]. In this perspective, the tunnel current is generated near the source/channel junction and can be characterized by a transfer of electrons and holes across this junction. Hence, the tunneling current for an electron with longitudinal energy $E$ and transverse energy $E_T$ can be expressed as follows [25]:

$$J(E)=\frac{q}{\pi h}\int\int T(E)\left[\left(f_l-f_r\right)\left(E+E_T\right)\right]\frac{\sqrt{m_e m_h}}{2\pi h^2}\mathrm{d}E\mathrm{d}E_T, \quad (1)$$

where $T$(E) represents the tunneling probability of the electrons, $q$ is the electron charge, $m_e$ and $m_h$ are the effective masses of electrons and holes, respectively, $h$ is the Planck constant. $f_l$ and $f_r$ are the Fermi–Dirac distributions on the left and the right side of the source/channel junction, respectively:

$$f_l(E)=\left[1+\exp\left(\frac{E+E_T-E_{fSiGe}}{k_BT}\right)\right]^{-1},$$
$$f_r(E)=\left[1+\exp\left(\frac{E+E_T-E_{fSi}}{k_BT}\right)\right]^{-1}, \quad (2)$$

where, $E_{fSiGe}$ and $E_{fSi}$ are the Fermi levels at the $Si_{1-x}Ge_x$ source and Si channel regions, respectively, $k_B$ is the Boltzmann constant and $T$ the temperature.

In order to reflect accurately the device behavior for very short dimensions like in our case, the modified drift–diffusion model, which includes other effects related to the short-channel nature of the investigated transistor and to quantum effects is used. Further, the gradient density model is also included, which consists of the quantum correction associated with the local potential to the carrier temperatures in the current equations [25]. Moreover, models for carrier recombination (Shockley–Read–Hall (SRH), Auger and surface recombination) are also adopted [26]. In fact, the carrier mobility mainly depends on three quantities, transverse and parallel electric field, doping and temperature, which were combined using Matthiessen's formula. Accordingly, the Lombardi model (CVT) is used to express the carrier mobility in the channel [27]. Moreover, the intrinsic parameters of the materials (Si, $Si_{1-x}Ge_x$ and Ge) such as band gap, mobility and the density of states were considered to be dependent on the Ge mole fraction ($x_{Ge}$). It should be noted that the *Ge* mole fraction is varied from 0 to 0.7. This corresponds to the experimental limit for growing $Si_{1-x}Ge_x$ when avoiding interfacial defects at the considered device thickness $t_{ch}$ = 5 nm [28].

## Results and Discussion

The main idea behind the proposed design is a modified heterostructured channel. In this context, it seems important to analyze the electrical behavior of the proposed design with considering different material configurations at the source, drain and channel regions in order to distinguish which heterochannel design provides the best electrical performance. Figure 2 depicts $I_{ds}$–$V_{gs}$ characteristics of the proposed design with different material configurations of the heterochannel compared to that of the conventional designs with $L_g$ = 20 nm, $L_s$ = 10 nm and $N_d$ = 1·10$^{19}$ cm$^{-3}$.

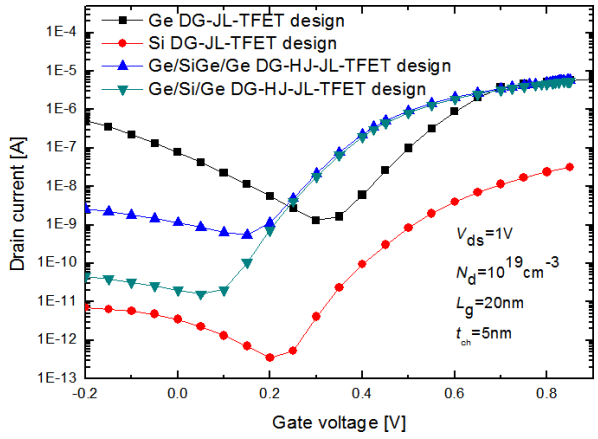



**Figure 2:** Drain current as a function of the applied gate voltage for the DG-HJ-JL TFET proposed with different heterochannel configurations compared to that of the conventional homochannel designs ($L_g$ = 20 nm, $L_s$ = 10 nm and $N_d$ = 1·10$^{19}$ cm$^{-3}$, $t_{ch}$ = 5 nm and $V_{ds}$ = 1 V).

The proposed DG-HJ-JL TFET design with Ge/Si/Ge channel structure exhibits better electrostatic behavior and less parasitic ambipolar conduction than the other designs. In fact, this behavior can be attributed to two essential effects: Firstly, the enhanced tunneling current resulting from the low tunneling barrier giving rise to a higher probability of electron transfer at the source/channel interface. Secondly, the heterostructure at the channel/drain interface can be beneficial for sufficiently enlarging the tunneling barrier under reverse-bias conditions in order to effectively suppress the undesired ambipolar conduction. Moreover, we can notice that the conventional design with Si channel shows a reduced OFF-state current compared to that of the investigated heterochannel designs, which is mainly due

to the high band-gap energy and the low electron mobility associated to Si. On the other hand, the conventional Ge-DG-JL TFET design provides higher ON-state current. This is due to the smaller band gap energy of Ge, yielding a higher tunneling efficiency. Moreover, the higher electron mobility of Ge (3900 $cm^2 \cdot V^{-1} \cdot s^{-1}$) contributes to the increased drain current at the threshold voltage as compared to the conventional design with silicon (1400 $cm^2 \cdot V^{-1} \cdot s^{-1}$) channel. A suitable choice of the channel material can offer the possibility of enhancing the $I_{ON}/I_{OFF}$ ratio as well as achieving a lower swing factor. For this purpose, introducing $Si_{1-x}Ge_x$ material at the source side can be useful for achieving an improved electrical behavior through modulating the tunneling barrier width at the source/channel junction by varying the Ge concentration.

Figure 3a shows the transfer characteristics associated of the proposed $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET design with different Ge mole fractions. Increasing the Ge content leads to an increase of the drain current. This is mainly due to the enhanced carrier mobility caused by the increased Ge content. Moreover, introducing SiGe at the source side can be effective for reducing the tunneling barrier. Besides, the Ge concentration increase induces a lowering of the tunneling barrier, which enables enhancing the derived current capability as shown in Figure 3a. It can be also concluded that the Ge mole fraction modulates the threshold voltage for the tunnel-current generation, which can in turn influence greatly the subthreshold behavior of the device. Moreover, the proposed $Si_{1-x}Ge_x$/Si/Ge heterochannel enables a superior control of the channel conductivity through modulating the electric field at the heterojunction interfaces. In this regard, it is of great importance to illustrate the electric field distribution for a better understanding of the physical rules governing the obtained improvements of the electrostatic behavior. Figure 3b compares the distribution of the electric field along the channel of the proposed $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET design to that of the conventional Ge-DG-JL TFET counterpart. Clearly, a considerable change in the electric field distribution can be achieved by including the heterochannel, with higher electric field arising in the source/channel interface as well as along the channel. This indicates that by a proper choice of the channel material, we can achieve an enhanced electrostatic behavior. This enables improving the carrier transport efficiency and thereby the device derived current capability at the nanoscale level.

In order to get a qualitative idea about the impact of the Ge concentration on the electrical performance of the proposed DG-HJ-JL TFET design, Figure 4a shows both $I_{ON}/I_{OFF}$ ratio and the subthreshold swing factor as functions of the Ge mole fraction. By increasing the Ge content, the $I_{ON}/I_{OFF}$ ratio increases significantly to reach its maximum for a Ge mole fraction value of 0.6 and saturates after this value. Moreover, the $I_{ON}/I_{OFF}$ ratio of the proposed DG-HJ-JL TFET is higher than that of the conventional structure with uniform channel. This can be attributed to the enhanced tunneling current resulting from the change of the tunneling barrier with increasing Ge content. Figure 4b compares the band diagrams of the DG-HJ-JL TFET design and the conventional structure with uniform Si channel. Figure 4b reveals that by introducing $Si_{1-x}Ge_x$, the tunneling barrier height at the source–channel junction decreases and a higher tunneling current can be generated when the band alignment at the junction is satisfied.

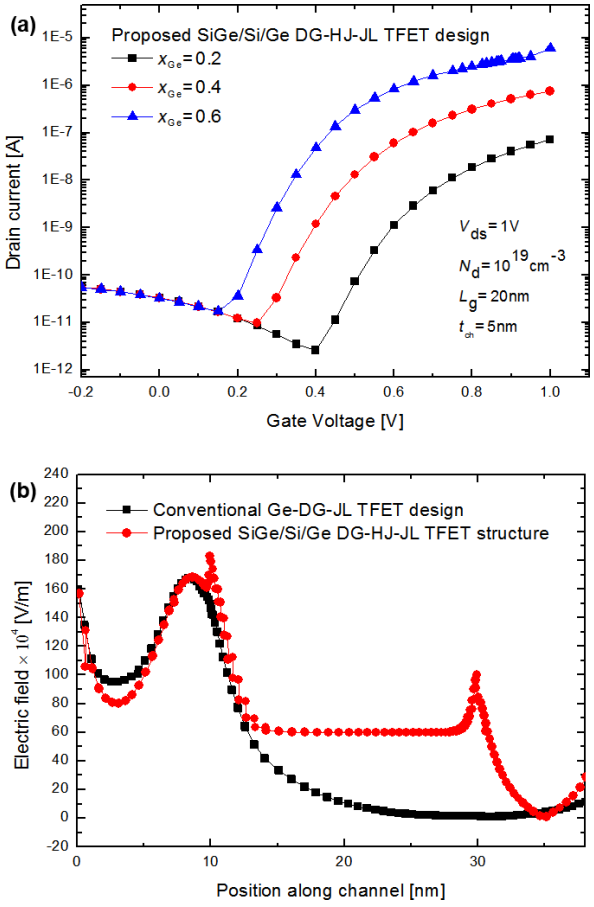



**Figure 3:** (a) Transfer characteristics of the proposed $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET as a function of the Ge concentration with $N_d$ = 1·10$^{19}$ cm$^{-3}$, $V_{ds}$ = 1 V, $t_{ox}$ = 2 nm, $L_g$ = 20 nm and $t_{ch}$ = 5 nm. (b) Distribution of the electric field along the channel of the proposed $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET structure and the conventional Ge-DG-JL TFET design with $N_d$ = 1·10$^{19}$ cm$^{-3}$, $t_{ch}$ = 5 nm, $t_{ox}$ = 2 nm, $L_g$ = 20 nm and $L_s$ = 10 nm.

In addition, Figure 4 shows the complex subthreshold behavior. The Ge mole fraction induces a highly non-linear behavior of the swing factor as it is shown in Figure 4a. This phenomenon can be ascribed to the quantum nature of the band-to-band tunneling effects, and determining the Ge concentration that

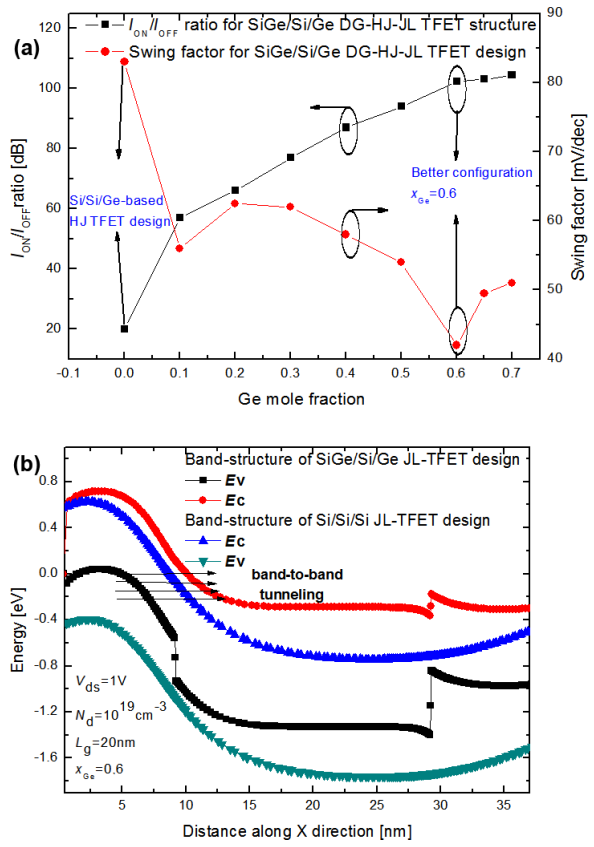



**Figure 4:** (a) Subthreshold swing factor and the $I_{ON}/I_{OFF}$ ratio as functions of the Ge mole fraction for the investigated $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET structure with $N_d$ = 1·10$^{19}$ cm$^{-3}$, $V_{ds}$ = 1 V, $t_{ox}$ = 2 nm, $L_g$ = 20 nm and $t_{ch}$ = 5 nm. (b) Comparison of the band diagrams of the proposed $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET design and the conventional structure with uniform Si channel.

provides an enhanced subthreshold behavior seems to be very complex at the nanoscale level. The swing factor decreases significantly above $x_{Ge}$ = 0.3, which can be explained by the effect of the tunneling barrier height on the device subthreshold behavior. At a Ge mole fraction of 0.6, a good trade-off between derived current capability and subthreshold behavior is obtained, with an $I_{ON}/I_{OFF}$ ratio value of 115 dB and a swing factor value of 42 mV/dec at the nanoscale level ($L_g$ = 20nm) as it is illustrated in Figure 4a.

More importantly, we analyze the impact of the optimized $Si_{1-x}Ge_x$/Si/Ge heterochannel structure on the device scaling capability for high-performance nanoelectronic applications. Figure 5 depicts the swing factor as a function of the transistor channel length for both the proposed $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET design and the conventional Ge-DG-JL TFET structure with $t_{ch}$ = 5 nm, $x_{Ge}$ = 0.6 and $N_d$ = 1·10$^{19}$ cm$^{-3}$. The optimized design provides better scaling capability than the conventional one and exhibits a faster decrease of the swing factor as a

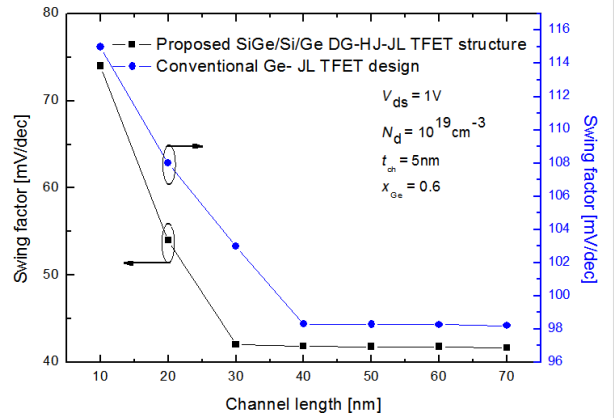



**Figure 5:** Subthreshold swing factor as a function of the channel length for both the proposed $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET and the conventional Ge-DG-JL TFET with $N_d$ = 1·10$^{19}$ cm$^{-3}$, $V_{ds}$ = 1 V, $t_{ox}$ = 2 nm, $L_s$ = 10 nm and $t_{ch}$ = 5nm.

function of the channel length. This behavior can be explained by the improved electrostatic response offered by the heterochannel.

For the completeness of this work, we analyze the improvements of the proposed design compared to conventional TFET devices with regard to the electrical performance. Table 1 summarizes an overall comparison of electrical metrics between the proposed $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET, the conventional Ge-DG-JL TFET design and the numerical results associated to the conventional Si-DG-JL TFET [18]. it reveals that the proposed design with heterochannel outperforms considerably the conventional counterparts, with 58% improvement regarding the subthreshold swing factor and 54% enhancement in terms of the $I_{ON}/I_{OFF}$ ratio. The optimized design improves the device tunneling performance, not only through a more effective carrier-transport mechanism, but also through a distinctive reduction of the undesired ambipolar conduction.

## Conclusion

In this work, a new DG-JL TFET design with a heterochannel ($Si_{1-x}Ge_x$/Si/Ge) has been proposed as a new way to achieve enhanced electrical performance and suppressed ambipolar conduction. It has been concluded from the obtained results that the investigated DG-HJ-JL TFET design offers the possibility to overcome the trade-off between improved switching characteristic and superior derived current capability. In addition, the impact of the Ge concentration on the electrical behavior of the device has been analyzed. It has been deduced that the proposed design with 60% of Ge provides an $I_{ON}/I_{OFF}$ ratio of 115 dB and a swing factor of 42 mV/dec. It has been also concluded that the optimized design offers superior scaling capability compared to the conventional Ge-DG-JL TFET structure.

**Table 1:** Overall electrical comparison of FoMs.

| | conventional Ge-DG-JL TFET design | proposed $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET structure | conventional Si-JL TFET structure [18] |
|---|---|---|---|
| design variables | | | |
| channel length $L_g$ (nm) | 20 | 20 | 20 |
| source/drain extensions length $L_{s/d}$ (nm) | 10 | 10 | 25 |
| dielectric permittivity | 25 | 25 | 25 |
| oxide thickness $t_{ox}$ (nm) | 2 | 2 | 2 |
| channel thickness $t_{ch}$ (nm) | 5 | 5 | 5 |
| gate work function (eV) | 4.3 | 4.3 | 4.3 |
| gated source work function (eV) | 5.6 | 5.6 | 5.9 |
| channel doping concentration $N_d$ ($cm^{-3}$) | $1{\cdot}10^{19}$, n-type | $1{\cdot}10^{19}$, n-type | $1{\cdot}10^{19}$, n-type |
| drain voltage $V_{ds}$ (V) | 1 | 1 | 1 |
| Ge mole fraction of $Si_{1-x}Ge_x$ source | — | 60 | — |
| performance parameters | | | |
| subthreshold swing (mV/dec) | 114 | 42 | 81 |
| $I_{ON}/I_{OFF}$ ratio (dB) | 79 | 115 | 98 |
| ambipolar conduction | high | suppressed | high |

Therefore, the optimized design opens up the route for achieving an enhanced derived current capability with suppressed ambipolar conduction and for improving the device subthreshold behavior at the nanoscale level. This makes the optimized $Si_{1-x}Ge_x$/Si/Ge DG-HJ-JL TFET design a potential alternative for high-performance nanoelectronic applications. Moreover, this study can be extended by investigating the impact of other parameters such as the interfacial defects between both Si and SiGe materials and the degradation-related ageing effects including stress. To do so, new complex models and numerical simulations need to be developed.

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# Electrical characterization of single nanometer-wide Si fins in dense arrays

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## Abstract

This paper demonstrates the development of a methodology using the micro four-point probe (μ4PP) technique to electrically characterize single nanometer-wide fins arranged in dense arrays. We show that through the concept of carefully controlling the electrical contact formation process, the electrical measurement can be confined to one individual fin although the used measurement electrodes physically contact more than one fin. We demonstrate that we can precisely measure the resistance of individual ca. 20 nm wide fins and that we can correlate the measured variations in fin resistance with variations in their nanometric width. Due to the demonstrated high precision of the technique, this opens the prospect for the use of μ4PP in electrical critical dimension metrology.

## Introduction

The transition from planar to three-dimensional transistor architectures such as the fin field-effect transistor (finFET) [1] has raised the need for measuring the electrical properties of nanometer-wide conducting features [2]. Recently, it has been shown that the micro four-point probe (μ4pp) technique, which is commonly used for sheet resistance measurements on blanket materials or relatively large pads (larger than 80 × 80 $\mu m^2$) [3-5], provides a solution to this requirement [6]. The μ4pp technique was demonstrated to provide (sheet) resistance measurements in single fins without the need for dedicated Kelvin resistor or transmission line structures [7]. However, the results demonstrated in [6] focused on isolated fins whereby the fin pitch was

larger than the contact size of the µ4pp electrodes such that only one single fin was contacted at a time. Intuitively, this suggests that the technique developed therein fails when trying to measure dense structures where a fin pitch smaller than the apparent contact size of the electrodes is used (see below in Figure 2). In that case, the µ4pp technique appears to be of limited value in routine semiconductor manufacturing where state-of-the-art chips use much smaller fin pitches [8].

In this paper, we describe further developments of the µ4pp technique, as implemented by the CAPRES A300 tool, which enable the electrical characterization of single nanometer-wide fins in dense fin arrays (pitch < 200 nm) with high precision and repeatability. First, we describe the general concept of how to establish and control the electrical contact between the metallic (Ni-coated) µ4pp electrodes and the semiconducting (Si) fins. Next, we show that, by carefully controlling this process, the electrical contact can be confined to one single fin such that the resistance of individual fins in dense arrays can be measured with a high precision. Finally, we use the technique to determine the electrical resistance of individual fins in a dense array and we demonstrate that the measured resistance correlates with the geometrical width of the fins, as measured with transmission electron microscopy (TEM). Due to the demonstrated high precision, a critical dimensional sensitivity of ca. 0.5 nm could be achieved.

## Experimental

Before discussing the electrical contact between the µ4pp electrodes and an individual fin, a general description of a µ4pp measurement on large blanket semiconducting samples is needed. The µ4pp electrodes comprise four Ni-coated Si cantilevers with a spacing of 8 µm and a contact size $d_{contact} \approx 300$ nm [6,9,10]. In a µ4pp measurement, the electrodes are landed on the sample surface after which a current $I_{in}$ is injected into the investigated sample via two of the electrodes while the induced voltage drop $V$ is measured between the other two electrodes. Initially, however, the native oxides present both on the semiconducting material and the Ni-coated electrodes act as highly resistive barriers and therefore prevent any electrical contact [11]. To establish the electrical contact, the µ4pp technique uses the so-called punch-through current, i.e., a short current pulse of magnitude $I_{pulse}$ applied between two electrodes, which causes the breakdown of the native oxide barrier [12-14] and hence creates the conductive path required to inject $I_{in}$ into the investigated material. Empirically, it is observed that the magnitude of $I_{pulse}$ must be chosen larger than a certain threshold current ($I_{threshold}$, typically >100 µA for blanket materials) in order to reduce the contact resistance $R_C$ between the electrodes and the sample and hence activate the required electrical contact.

The given description of the punch-through mechanism is also valid for more confined structures, such as fins. This does, however, require some additional considerations, starting with the distinction between isolated and dense fins. First, for isolated fins (Figure 1a), i.e., fins are separated by a distance (= pitch) larger than $d_{contact}$, the procedure is identical to the previously described case of blanket materials. The electrical contact is indeed created, i.e., contacts $j$ = 1, 2, 3, 4 are activated, when $I_{pulse} \geq I_{threshold}$ and the electrical resistance $R_{fin}$ of the region of the fin included between the two inner contacts is readily obtained from the ratio $R_{fin} = V/I_{in}$ [6]. Secondly, in the more complex case of dense fins, i.e., fin pitch < $d_{contact}$, the µ4pp electrodes can physically contact multiple fins at the same time. For simplicity, this paper only considers the case of two fins physically contacted by the electrodes (Figure 1b). In this situation, electrical contact is formed on both fins, i.e., contacts $j$ = 1, 2, …, 8 are activated, when the magnitude of $I_{pulse}$ is similar as used on blanket materials. The measured resistance is then determined by the ratio between the two currents $I_{in1}$ and $I_{in2}$ injected into the two electrically connected fins. Since this ratio depends on the contact resistances $R_{Cj}$ ($j$ = 1, 4, 5, 8), this leads to a high measurement variability, i.e., a loss in precision [3]. As a consequence, in order to precisely determine $R_{fin}$ in a dense fin array, $I_{pulse}$ should be carefully controlled ($I_{pulse} < 2 \times I_{threshold}$) to only allow for the formation of electrical contact to one single fin, i.e., only contacts $j$ = 1, 2, 3, 4 or $j$ = 5, 6, 7, 8 are activated. On top of that, to make sure that all four electrodes indeed form electrical contact with the same fin, the punch-through mechanism between electrode pairs must be

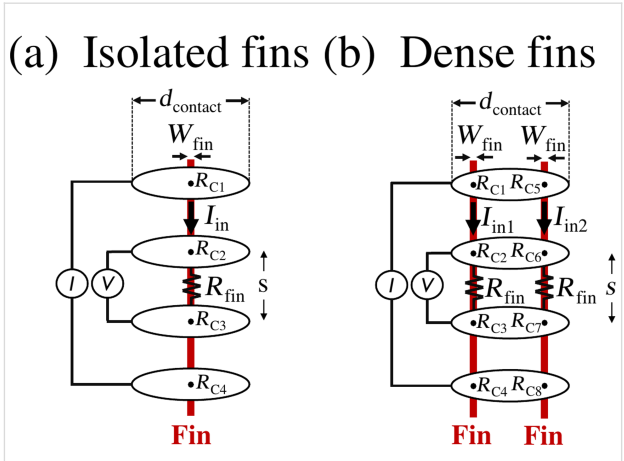



**Figure 1:** Top-view schematic of the four µ4pp electrodes landed on (a) a single fin and (b) two fins. The electrode contact size and the contact resistance for each electrode–fin contact are, respectively, indicated by $d_{contact}$ and $R_{Cj}$ ($j$ = 1, 2,…, 8). Note that all contact resistances are initially considered to be highly resistive because the native oxides present on both the fins and electrodes prevent current flow into the fin. $R_{fin}$ is defined as the resistance of the fin between the two inner contacts, i.e., $R_{fin} = R_s \times s/W_{fin}$, where $s$ is the distance between the two inner contacts and $W_{fin}$ is the fin width.

sequenced properly. For example, when first applying the punch-through mechanism on the top two electrodes, which then form electrical contact with the left fin in Figure 1b, i.e., contacts $j = 1$ and $j = 2$ are activated, the next electrode pair should use an already activated contact to make sure the contacts on the same fin, i.e., $j = 3$ or $j = 4$, are activated next. Note that, however, the exact behavior of the electrical contact formation on dense fins is still not fully understood and a more thorough description would also include pulse duration, peak voltage, and material properties.

## Results and Discussion

The experimental demonstration of using the punch-through current $I_{pulse}$ to individually contact single Si fins in dense arrays is shown in Figure 2a, where the measured $R_{fin}$ is plotted as a function of the fin width $W_{fin}$ after using a high (100 µA) or low (25 µA) punch-through current to form the electrical contact. To highlight the impact of the fin pitch, we have additionally separated the isolated and dense fins, assuming the approximately 300 nm physical contact size of the electrodes as measured with scanning electron microscopy (SEM) [9]. It can be observed that, while $I_{pulse}$ does not affect the precision on isolated fins (red and blue triangles), for dense fins a major improvement in precision can be achieved by decreasing the punch-through current from 100 µA (red diamonds) to 25 µA (blue diamonds). Based on the previous theoretical considerations, the improvement in precision is achieved by restricting the electrical contact to one single fin despite the electrode being in physical contact with two fins. To show this improvement more clearly, the relative standard deviation of the measured values of $R_{fin}$ can be plotted against the fin pitch, as shown in Figure 2b. Excitingly, the precision of the 25µA punch-through current measurement remains stable at around 3%, making the measurement feasible even for fin pitch much smaller than $d_{contact}$. Note that Figure 2 also shows that the fin width has no impact on the measurement precision.

The ability to probe individual fins in dense arrays allows us to exploit the high precision of the µ4pp tool [15] to electrically characterize nanometer-wide fins regardless of the fin pitch. To demonstrate this, Figure 3 shows that we can now measure variations in fin resistance induced by nanometric variations in fin width in a dense array of narrow Si fins. For this, we used an array of ten ca. 20 nm wide Si fins implanted with B ($3 \times 10^{15}$ cm$^{-2}$, 5 kV) and laser-annealed three times at 1150 °C. Note that $W_{fin}$ is assumed constant, i.e., the very small tapering of the fins along the shallow (ca. 60 nm) implant depth [6] is ignored. These fins, having a pitch of 200 nm, were measured individually by using a punch-through current of 25 µA to restrict the electrical contact to a single fin. Moreover, by running the µ4pp measurement over the fin array with a step size of ca. 25 nm, we could assign the measured values of $R_{fin}$ to each specific fin. As can be observed for the four out of ten fins shown in Figure 3a, $R_{fin}$ varies in accordance with the fin width measured by TEM. Note that the error in Figure 3a is 3.0% for each fin, which was obtained by taking the lowest precision achieved out of all ten measured fins. Since $R_{fin}$ is obtained by taking the average of several subsequent measurements, the precision includes the variation in the exact position of the electrical contact points for each landing of the electrodes, i.e., a variation in contact spacing $s$, which may result both from a variation in the electrode positioning itself and from the exact location of the small electrical contact under the wider electrode. Additionally, using the widths measured with TEM

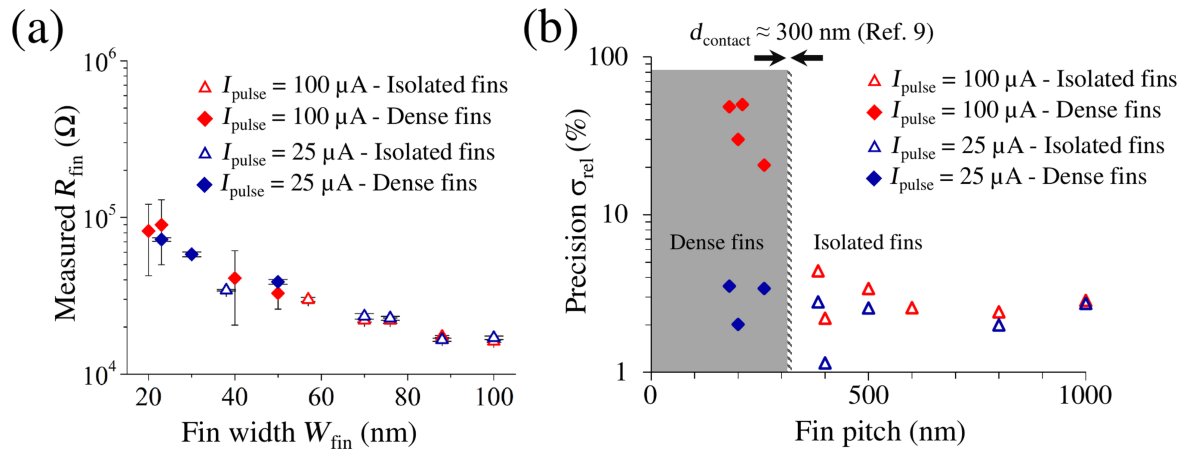



**Figure 2:** (a) Measured fin resistance $R_{fin}$ as a function of fin width $W_{fin}$ on isolated (triangle) and dense (diamond) fins using high (red) and low (blue) punch-through currents. (b) Relative standard deviation of the measured values of $R_{fin}$ of Figure 2a as a function of the fin pitch. When using a low punch-through current (blue), the relative standard deviation remains stable (≤3%) regardless of fin pitch, indicating that the electrical contact remains restricted to a single fin, even in the grey area where the electrodes are in physical contact with more than one fin.

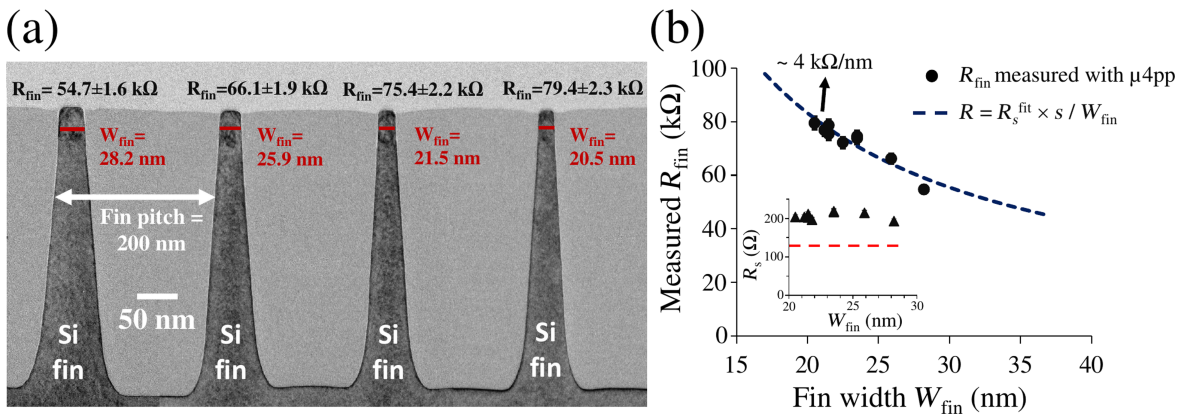



**Figure 3:** (a) TEM image of four ca. 20 nm wide Si fins where the measured $R_{fin}$ is indicated on top of each fin. The measured values of $R_{fin}$ correlate to the respective fin width $W_{fin}$ according to $R_{fin} = R_s^{fin} \times s/W_{fin}$. The error for each fin refers to the lowest precision (3.0%) achieved on all measured fins. (b) Measured fin resistance as a function of $W_{fin}$ fitted to a constant sheet resistance $R_s^{fin}$ using the relation $R_{fin} = R_s^{fin} \times s/W_{fin}$ (using $s$ = 8 µm). The slope of the fitted curve at $W_{fin}$ = 20 nm is indicated (ca. 4.0 kΩ/nm). (inset) Sheet resistance ($R_s^{fin}$) of the ten Si fins obtained using the inversed relation $R_s^{fin} = R_{fin} \times W_{fin}/s$, plotted against fin width $W_{fin}$. For comparison, the dashed red line shows the low sheet resistance $R_s^{pad}$ = 135 Ω measured on a large pad of the same material as the fins.

and the relation $R_{fin} = R_s^{fin} \times s/W_{fin}$ (using $s$ = 8 µm), the inset of Figure 3b shows that all ten fins have the same sheet resistance $R_s^{fin} \approx 200$ Ω/sq, indicating that the observed variations in $R_{fin}$ are indeed caused by variations in fin width. This allows us to evaluate the sensitivity of the technique by plotting the measured values of $R_{fin}$ as a function of the fin width (Figure 3b) and subsequently fitting the data with a constant sheet resistance $R_s^{fin}$ using the relation $R_{fin} = R_s^{fin} \times s/W_{fin}$. By comparing the slope of the fitted curve at $W_{fin}$ = 20 nm (ca. 4 kΩ/nm) to the achieved precision (ca. 2.3 kΩ, Figure 3a), we can deduce that the technique has a sensitivity to variations in fin width down to about 0.5 nm, opening the prospects for its use in electrical critical dimension metrology. As also interestingly shown in the inset of Figure 3b, the measured $R_s^{fin}$ is higher than the sheet resistance $R_s^{pad}$ = 135 Ω (dashed red line) measured in a large 80 × 80 µm$^2$ pad having undergone the same implantation and annealing treatment. This increase in sheet resistance when going to nanoscale elongated geometries was expected and understood to originate from the presence of interface states as well as defects at the fin sidewalls [6].

## Conclusion

This paper demonstrates the capability of µ4pp to electrically characterize individual nanometer-wide Si fins in dense arrays regardless of fin pitch. By carefully controlling the electrical contact, we were able to measure the resistance of individual ca. 20 nm wide fins in dense arrays even though the µ4pp electrodes physically contact more than one fin. Thanks to the high precision of the measurements, the correlation between measured resistance and nanometer-scale variations in fin width could be demonstrated with a sensitivity as small as 0.5 nm.

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# A differential Hall effect measurement method with sub-nanometre resolution for active dopant concentration profiling in ultrathin doped $Si_{1-x}Ge_x$ and Si layers

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## Abstract

In this paper, we present an enhanced differential Hall effect measurement method (DHE) for ultrathin Si and SiGe layers for the investigation of dopant activation in the surface region with sub-nanometre resolution. In the case of SiGe, which constitutes the most challenging process, we show the reliability of the SC1 chemical solution ($NH_4OH/H_2O_2/H_2O$) with its slow etch rate, stoichiometry conservation and low roughness generation. The reliability of a complete DHE procedure, with an etching step as small as 0.5 nm, is demonstrated on a dedicated 20 nm thick SiGe test structure fabricated by CVD and uniformly doped in situ during growth. The developed method is finally applied to the investigation of dopant activation achieved by advanced annealing methods (including millisecond and nanosecond laser annealing) in two material systems: 6 nm thick SiGeOI and 11 nm thick SOI. In both cases, DHE is shown to be a uniquely sensitive characterisation technique for a detailed investigation of dopant activation in ultra-shallow layers, providing sub-nanometre resolution for both dopant concentration and carrier mobility depth profiles.

## Introduction

The research efforts made throughout the last decades have made it possible to keep the momentum for a continuous miniaturization of electronics devices. For instance, the “bulk” planar transistor limitations have been overcome thanks to the transition towards more complex device architectures. These include enhanced planar architectures such as fully depleted silicon on insulator (FDSOI) [1] or 3D architectures ranging from TriGate FinFETs [2] to gate-all-around NWFETs [3] and monolithic 3D CoolCube technology [4]. Despite their differences, some technological issues have emerged as a significant challenge for all

of them, such as the need to reduce the contact resistance at the silicide/source–drain interface [5].

The increase of the active dopant concentration at the surface of the source/drain material (usually Si or SiGe) is a key factor for obtaining a resistance reduction [6], and several process solutions have been proposed to this purpose, involving advanced implanting or annealing techniques [7]. Within this context, the optimization of existing characterisation techniques for the measurement of dopant activation at the semiconductor surface (or the development of new ones) is therefore decisive for both the improvement of the fabrication processes and the calibration of the related technology CAD (TCAD) physical models.

For device architectures based on planar SOI substrates (such as FDSOI or 3D CoolCube), measurements of active dopant concentrations from "blanket wafer" experiments are still relevant for process and TCAD optimisation, which are in principle achievable thanks to several known 1D measurement techniques previously developed for dopant profiling. However, in the case of contact resistance optimisation, only the dopant concentration close to the surface is relevant, i.e., within the first few nanometres, while the SOI/SiGeOI substrates used in current technologies are extremely thin (top layer < 10 nm), making measurement techniques with sub-nanometre resolution necessary. 1D techniques based on small-angle bevel preparation (such as spreading resistance profiling (SRP) [8] or scanning capacitance microscopy (SCM) [9,10]) become extremely difficult to implement and control in view of such a small resolution. Thanks to the use of an AFM tip, 2D scanning spreading resistance microscopy (SSRM) has been shown to achieve sub-nanometre resolution [11,12]. However, in this technique, the carrier concentration is inferred from a resistivity profile under the assumption that carrier concentration varies ideally with mobility, which is not always the case, especially when a part of the dopant is not electrically active [13]. For this reason, reliable mobility and concentration profiling based on scanning probe techniques require a combination of resistivity measurements by SSRM with carrier concentration measurements by SCM [14]. Finally, capacitance-based techniques such as SCM or electrochemical capacitance voltage (ECV) [15], provide reliable values of carrier concentrations only in the absence of additional electrically active defects, which can affect the CV signal [16].

In contrast, differential Hall effect (DHE) profiling [17,18] can potentially meet all the requirements related to the precise measurement of dopant activation at the semiconductor surface. DHE relies on the iteration of etching process and conventional Hall effect measurements. The active carrier profile is therefore measured without any assumption about the magnitude of the carrier mobility. In addition, measurements are made by stripping the material in successive steps rather than bevelling the surface. The depth resolution of the final dopant concentration profile is therefore defined by the etch rate and indeed nanometric resolution has been successfully demonstrated for Si and Ge, applying oxidation processes such as anodisation [19] or oxidising chemistry [20-23]. Nevertheless, etching SiGe alloys with nanometric resolution is far more challenging considering that Si and Ge have different oxidation rates [24]. For this reason, reliable DHE measurements of doped SiGe layers have not been reported in literature. Finally, in all published DHE investigations, the removal rate is assumed to stay constant. However, even small variations in the removed thickness among nominally identical etch steps can strongly distort the final carrier concentration and mobility profiles.

In this paper, we present an enhanced differential Hall effect measurement method that allows to precisely determine the level of dopant activation close to the semiconductor surface for Si and SiGe. First, we detail the etching processes that we have developed for each semiconductor, with particular focus to the SiGe case, which constitutes the most challenging process. For both materials, our method includes a direct measurement of the removed thickness after each removal step, so to avoid averaging the etch rate and improve the accuracy of final calculated values. Then, we demonstrate the reliability of a complete DHE procedure on a dedicated SiGe test structure fabricated by CVD and uniformly doped in situ during growth. Finally, we will apply our DHE method to the investigation of dopant activation achieved by advanced annealing methods in two material systems: 6 nm SiGeOI and 11 nm SOI.

## Development of Etching Processes for $Si_{1-x}Ge_x$ and Si

### Etching process for $Si_{1-x}Ge_x$

Different methods have been proposed in literature for the controlled etch of SiGe layers [25-27]. We first analysed the main characteristics of each solution in terms of the specific requirements related to their application for DHE measurements. In particular, (i) the solution must etch Si and SiGe simultaneously so that the SiGe stoichiometry is not modified; (ii) the solution must be strongly selective with respect to Si so to preserve the surrounding Si areas in Van der Pauw test structures; (iii) the solution must be chemically active for a relatively long period (about 1 day) so to be used for several "etch and measurement" cycles; (iv) the etch rate must be slow (ca. 1 Å·min$^{-1}$) to allow for sub-nanometre resolution. Taking into account the above mentioned criteria, we therefore selected the one-step chemistry based on SC1 ($NH_4OH/H_2O_2/H_2O$

1:1:5), which oxidizes and removes both materials at the same time.

We then investigated the efficiency of the SC1 solution by running several tests as a function of different experimental parameters including time, temperature and Ge content. For this, spectroscopic ellipsometry (with a HORIBA Jobin Yvon system) was used as a fast, reliable and non-destructive method for the measurement of the removed thickness. We developed an empirical model for the quantification of the SiGe thickness measurement (based on a SiGe/Si two layers stack and a point-by-point calculation procedure), which was calibrated using other techniques (such as TEM and XRD). As an example, Figure 1 summarizes the removed thickness measured by XRD (in (004) configuration), high-resolution TEM and ellipsometry as a function of the etching time of a 20 nm thick $Si_{0.73}Ge_{0.27}$ boron-doped layer ($10^{18}$ $cm^{-3}$) grown on top of a Si substrate.

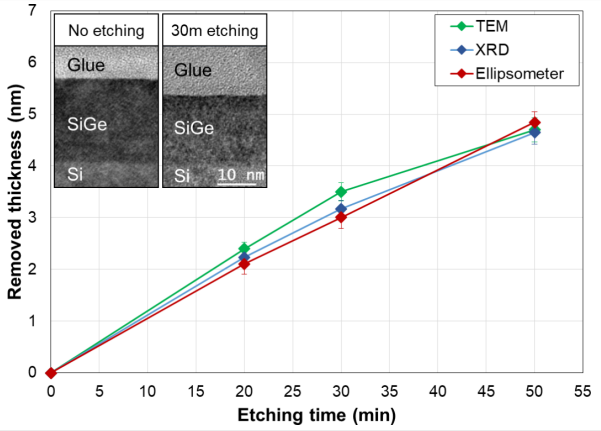



**Figure 1:** Removed SiGe thickness measured by different methods (TEM, XRD and ellipsometry) as a function of the etching time. Ge content: 27 atom %. Inset: TEM cross-section micrographs of reference and the sample etched for 30 min. This figure illustrates the agreement between the three chosen techniques.

TEM images show a clear decrease of the layer thickness, while all the techniques are in mutual agreement, therefore validating ellipsometry as a unique thickness characterization method for the remainder of this work. From this study we estimated a value of 0.95 Å·$min^{-1}$ for the etch rate of the SC1 solution on $Si_{0.73}Ge_{0.27}$, without any alteration of the initial layer stoichiometry, as confirmed by XRD analysis (Figure S1, Supporting Information File 1). Moreover, the found etch rate is in very good agreement with previous results obtained by our research group [26]. Concerning the surface roughness, tapping mode AFM analysis provided arithmetic averages $R_a$ of about 1.2 Å (Figure S2, Supporting Information File 1).

However, in view of its application for DHE experiments, it is necessary to use an encapsulation cell to protect metallic contacts of the electric test structures during etch (Figure S3, Supporting Information File 1). Due to the funnel-shaped cell designed for this study, the reaction zone is confined, which results in a reduction of the etch rate. By optimising the experimental set up (use of a magnetic stirrer combined with an appropriate cell orientation in the solution bath), we managed to limit the etch rate reduction and similar values to experiments with "blanket" samples were found. Finally, we investigated the impact of the Ge content on the measured etch rate. The results are shown in Figure 2, where we compare the removed thickness as a function of the etching time for two 20 nm boron-doped ($10^{19}$ $cm^{-3}$) $Si_{1-x}Ge_x$ samples with different germanium content : $x$ = 0.22 and $x$ = 0.30. For etching times less than 15 min, the etch rate is perfectly linear and independent of the Ge content, with a removed thickness of ca. 1 nm after 15 min. It is therefore possible to use this solution to achieve sub-nanometre resolution. In summary, all these investigations confirm the choice of SC1 as chemical solution for SiGe etching because of its slow etch rate, stoichiometry conservation and low roughness generation.

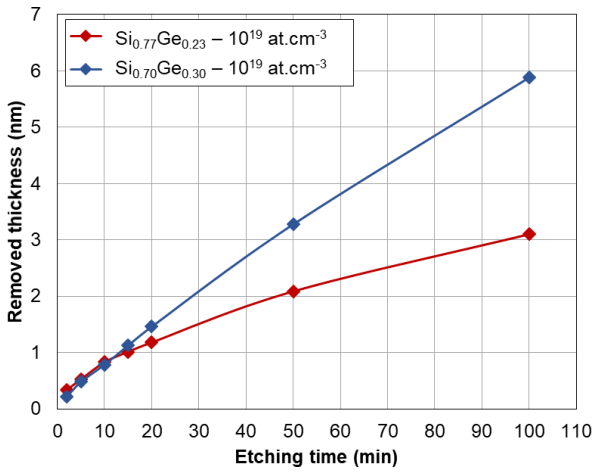



**Figure 2:** Removed SiGe thickness (measured by ellipsometry) as a function of etching time for two different Ge contents. After the first 15 min, the etch rate increases with Ge content.

## Etching process for Si

The silicon etching process differs from the etching of SiGe insofar as it involves a two-step mechanism: first, oxidation and then oxide stripping. In this case, the etch rate is not defined as a function of the etching time, but is given by the removed thickness per step, i.e., the removed thickness between two stripping processes. A resolution of about 1 nm has been obtained in the study of Ling et al. [22] combining dilute HF, ultrapure water rinsing and re-oxidation in a clean-room environment. However, with the aim of minimising the surface roughness, we used ethanol instead of ultrapure water as rinsing

solvent [28]. We performed multiple cycles of etching processes on in situ boron-doped Si layers (grown on top of Si substrates) with continuous monitoring of the removed thickness (by ellipsometry measurements) and the surface roughness (by AFM characterization). Our results show a cycle-by-cycle etch rate below 1 nm and a final roughness of 1 Å.

## DHE procedure validation on SiGe layers fabricated by CVD

In this section, we detail a complete DHE procedure using a 20 nm thick boron-doped ($10^{19}$ $cm^{-3}$) $Si_{0.77}Ge_{0.23}$ layer grown by CVD on top of a Si substrate. We first describe the Van der Pauw structure and the conventional Hall effect setup. Then we will present the differential Hall effect measurements and calculations and we will discuss the limitations of the technique.

## Van der Pauw structure and Hall effect measurements on ultrathin layers

The Hall effect measurement is a well-known technique that allows one to access three important physical parameters for material characterization: the sheet resistance $R_s$, the active Hall dose $N_H$ and the Hall mobility $\mu_H$. At first, a Van der Pauw technique is used to determine the sheet resistance, then a magnetic field is applied orthogonally to the sample surface to measure the sheet Hall coefficient $R_{SH}$, which is finally used to deduce $N_H$ and $\mu_H$.

Several classical Van der Pauw shapes were tested to perform electrical measurements (square, Greek cross and bridge "bar-shaped" structures). A test structure in the form of a Greek cross has been chosen as it has more advantages than other shapes (Figure S4, Supporting Information File 1). First, it provides an error of less than 1% on both sheet resistance and Hall coefficient measurements [29-32]. Moreover, it has a highly symmetrical shape with peripheral contacts separated from the centre region, in which the current lines converge allowing precise characterization. For this last reason, we were able to design an encapsulation cell (Figure S3, Supporting Information File 1) defining a reaction region in the centre part of the Greek-cross structure while protecting the metallic contacts with the lowest impact on structure symmetry and measurement reproducibility.

Electrical measurements were carried out with a HL5500PC Nanometrics Hall bench equipped with a 0.3 T magnet. For each investigated sample, the sheet resistance and the Hall coefficient were measured for several values of the injected current (from 1 μA to 1 mA), and the average values were determined within the current interval exhibiting the most stable measurements (Figure S5, Supporting Information File 1), so to keep the experimental errors close to 0.1%.

Scattering correction must be accounted for when extracting Hall effect parameters. The measured values of Hall carrier concentration and Hall mobility are therefore corrected by using the Hall scattering factor, $r_H$, [33-35] which depends on the studied material, i.e., on Ge content, doping type and concentration. For this study, we used a set of dedicated test samples consisting of 20 nm thick epitaxially grown Si and SiGe layers, in situ doped with boron (from $1 \times 10^{18}$ $cm^{-3}$ to $1 \times 10^{20}$ $cm^{-3}$). By comparing experimental Hall values with average calculated values based on the dopant concentration profiles measured by SIMS, we determined a scattering factor of 0.75 for holes in Si and values ranging from 0.4 to 0.35 for holes in SiGe with a Ge content of 22 atom % and 30 atom %, respectively, in perfect agreement with literature (Figure S6, Supporting Information File 1) [33-35].

Some other possible limitations should be considered in view of the implementation of a DHE methodology on ultrashallow layers. One is quantum confinement, which has been shown to induce band modifications in ultrathin SOI layers with thicknesses close to ca. 3 nm [36]. However, the SOI and SiGeOI layers to be investigated in this work will have a minimum thickness of about 6 nm, so that the quantum-confinement effect can be neglected. An additional low-dimension effect is the dielectric confinement, which has been investigated in silicon nanowires surrounded by a dielectric material (such as its native oxide) [37,38]. For nanowire diameters of about 10 nm, a dopant deactivation is observed due to the dielectrical mismatch between the silicon and its surroundings. However, our previous investigations on 5 nm thick SiGeOI layers doped by ion implantation and activated by conventional rapid thermal annealing (RTA) [39,40] indicated a perfect correlation between measured activation and simulated activation, suggesting that dielectric confinement affects more significantly 3D than 2D structures at low dimensions.

Finally, when quantifying the active dopant and mobility depth profiles with DHE, the surface-depletion effect should be considered [41,42]. This results from carriers becoming trapped in surface states and can lead to a depletion of carriers below the surface. As a consequence, the DHE profile might require a correction (depth-scale translation) corresponding to the depletion width. And in the case of non-uniform doping profiles, the depletion width (and the related correction) will vary with depth. For example, in the particular case discussed in this section, the investigated 20 nm thick SiGe layer is uniformly doped at $10^{19}$ $cm^{-3}$. For typical silicon-dioxide charge densities of $10^{12}$ $cm^{-2}{\cdot}eV^{-1}$, simple calculations provide a depletion width of about 2 nm. Consequently, in this case, a depth-scale translation is necessary. However, for the higher carrier concen-

trations typically investigated in source/drain doping studies, such as those discussed in the next section ($10^{20}$ cm$^{-3}$ and above), and considering the same typical silicon-dioxide charge densities, the surface depletion is well below 1 nm (about 0.4 nm at $10^{20}$ cm$^{-3}$ and less than 0.2 nm at $5 \times 10^{20}$ cm$^{-3}$; Figure S7, Supporting Information File 1) and its impact on the quantification of the DHE depth profiles can therefore be neglected.

## Differential Hall effect data measurements and limitations

We performed a full set of DHE measurements on a 20 nm thick $Si_{0.77}Ge_{0.23}$ layer grown by CVD on top of Si a substrate and uniformly doped with boron at $10^{19}$ cm$^{-3}$ (Figure S8, Supporting Information File 1). The layer was verified to be fully electrically active. A first run of six etch cycles (15 min each) was initially performed. The sample was then kept for three days in a clean room environment. Then, a second run of three etch cycles was carried out. Both runs were initiated without removing the initial native silicon dioxide. Electrical parameters $R_S$, $N_H$ and $\mu_H$ are reported in Figure 3 as a function of the etching time. Error bars are not reported as variations for each measured parameter are close to 0.1% (Figure S5, Supporting Information File 1).

Two different effects are observed. On one hand, the mobility stays constant with no discontinuity throughout the two measurement runs. On the other hand, the sheet resistance $R_S$ constantly increases (while the Hall dose $N_H$ decreases) and exhibits a discontinuity between the two runs. Indeed, as the doping concentration is uniform throughout the doped layer, the associated carrier mobility is expected to remain invariant in the entire layer. In contrast, as the layer becomes thinner and thinner, the active Hall dose decreases and, for a fixed carrier concentration (and hence mobility), the increase of the sheet resistance is predicted by Equation 1:

$$R_S = \frac{1}{q\int_0^{X_j} C(x)\mu(x)\,dx}, \quad (1)$$

with $X_j$ being the layer thickness, $q$ the electronic charge, $C(x)$ the dopant concentration as a function of depth and $\mu(x)$ the corresponding mobility profile. The quasi-linear evolution of both $R_S$ and $N_H$ is therefore due to the combination of a uniform concentration profile and constant etching time intervals. Concerning the observed discontinuities, it must be considered that a regrowth of native oxide occurs between the last measurement of the first run and the first measurement of the second one. This regrowth reduces the SiGe thickness by about 1 nm (as measured by ellipsometry), which results in a sheet resistance increase and a decrease of the active Hall dose, without influencing the mobility.

Starting from these raw data, it was finally possible to calculate the differential values of the active concentration and mobility as a function of the depth. For the $i$-th etched layer, the calculated values are defined by the following equations [16]:

$$n_{DHE_i}\left(x+\frac{\Delta x_i}{2}\right) = \frac{r_H}{q\Delta x_i}\frac{\left[\Delta(\sigma_S)_i\right]^2}{\Delta\left(R_{SH}\sigma_S^2\right)_i}, \quad (2)$$

$$\mu_{DHE_i}\left(x+\frac{\Delta x_i}{2}\right) = \frac{\Delta\left(R_{SH}\sigma_S^2\right)_i}{r_H\Delta(\sigma_S)_i}, \quad (3)$$

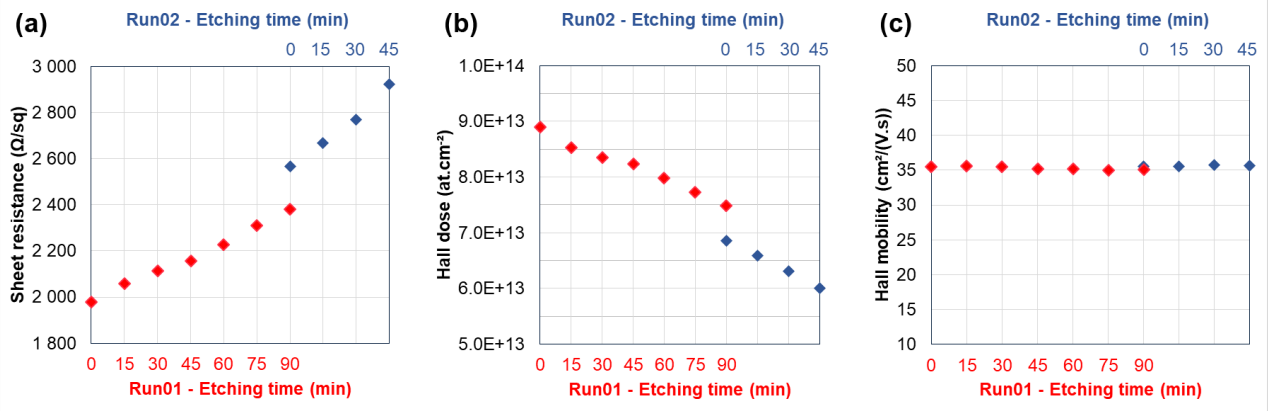



**Figure 3:** (a) Sheet resistance $R_S$, (b) Hall dose $N_H$, and (c) Hall mobility $\mu_H$ as functions of the etching time for a 20 nm thick SiGe layer ($x_{Ge}$ = 0.23) grown by CVD and in situ doped with boron.

with

$$\sigma_S = 1/R_S,$$
$$\Delta x_i = x_{i+1} - x_i,$$
$$\Delta(\sigma_S)_i = \sigma_{S_{i+1}} - \sigma_{S_i},$$
$$\Delta\left(R_{SH}\sigma_S{}^2\right)_i = \left(R_{SH}\sigma_S{}^2\right)_{i+1} - \left(R_{SH}\sigma_S{}^2\right)_i,$$

where the conductivity $\sigma_S$ is given by inversing the measured values of the sheet resistance $R_S$, and $R_{SH}$ is the sheet Hall coefficient used to extract the Hall dose and carrier mobility for each measurement. The term $\Delta x_i$ corresponds to the removed thickness after each etching process, which is determined by ellipsometry.

From Equation 2 and Equation 3, DHE profiles of active dopant concentration and mobility are finally deduced and reported in Figure 4a and Figure 4b, respectively (red diamonds). The active dopant concentration profile is compared in Figure 4a with the chemical dopant profile measured by SIMS (blue dots). The comparison is made assuming a constant depletion width of 2 nm for each DHE measurement (in agreement with the uniform doping level of the investigated sample). Blue solid lines represent the possible error (±12.5%) of the SIMS concentration values quantified from standards. It has to be noted that the SIMS signal in the first nanometres below the surface is affected by measurement artefacts and cannot be considered as fully reliable. Also, at the beginning of each of the two measurement runs, the presence of a native oxide at the sample surface may result in a different electrostatic configuration of the surface compared to all other cases where the electrical measurements are performed just after the SC1 etching step. This is probably the reason for the upward shift of the calculated concentrations at the surface (first point in Figure 4a) and at a depth of 5.5 nm. Overall, Figure 4a shows a very good correspondence between the SIMS and the DHE profiles, in perfect agreement with the full electrical activation of the doped layer. More importantly, we show that the SC1 chemistry allowed us to achieve a depth resolution of ca. 0.5 nm.

The horizontal error bars of the DHE values are solely related to the uncertainty of the thickness measurements done by ellipsometry (with the surface-depletion effect having been accounted for by a rigid shift of the depth scale). Indeed, by performing ellipsometry measurements after each removal step, any possible source of errors related to etch rate variation during the experiment can be neglected. The vertical error bars uncertainties of DHE mobility and dopant concentration ($S_{\mu DHE}$ and $S_{nDHE}$, respectively) calculated assuming $R_{SH}$, $\sigma_S$ (and the product $R_{SH}\cdot\sigma_S{}^2$) to be independent variables [17]:

$$S_{\mu_{DHE}} = \left[2\alpha_2{}^2\left(S_{R_{SH}}{}^2 + 4S_{\sigma_S}{}^2\right) + 2\alpha_1{}^2 S_{\sigma_S}{}^2\right]^{\frac{1}{2}}, \quad (4)$$

$$S_{n_{DHE}} = \left[2\alpha_2{}^2\left(S_{R_{SH}}{}^2 + 4S_{\sigma_S}{}^2\right) + 8\alpha_1{}^2 S_{\sigma_S}{}^2\right]^{\frac{1}{2}}, \quad (5)$$

with

$$\alpha_1 = \frac{\sigma_S}{\Delta\sigma_S}, \quad (6)$$

$$\alpha_2 = \frac{R_{SH}\sigma_S{}^2}{\Delta\left(R_{SH}\sigma_S{}^2\right)}, \quad (7)$$

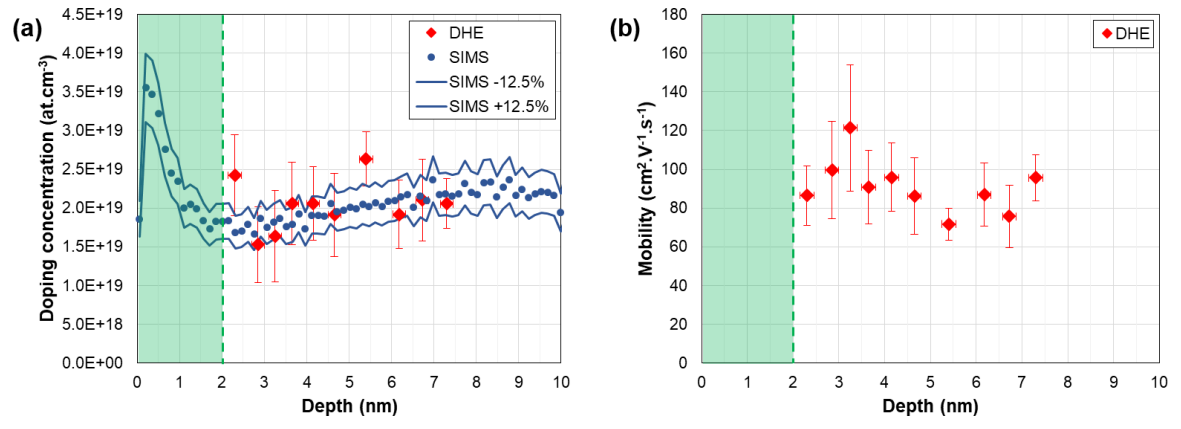



**Figure 4:** Depth profiles of (a) active dopant concentration and (b) carrier mobility extracted from the DHE measurements of $Si_{0.77}Ge_{0.23}$ uniformly boron-doped at $10^{19}$ $cm^{-3}$. In panel (a), the active dopant concentration profile is compared to the chemical boron concentration profile measured with SIMS. Green areas are depletion regions.

$$S_{R_{SH}} = \frac{100}{\left|\overline{R_{SH}}\right|}\sqrt{\frac{1}{n-1}\sum_{i=1}^{n}\left(\overline{R_{SH}} - R_{SH_i}\right)}, \quad (8)$$

$$S_{\sigma_S} = \frac{100}{\left|\overline{\sigma_S}\right|}\sqrt{\frac{1}{n-1}\sum_{i=1}^{n}\left(\overline{\sigma_S} - \sigma_{S_i}\right)}, \quad (9)$$

where $S_{RSH}$ (Equation 8) and $S_{\sigma S}$ (Equation 9) represent the relative standard deviations of $R_{SH}$ and $\sigma_S$ calculated in the range of stability (Figure S5, Supporting Information File 1). It is interesting to note that for a chosen etching time interval, i.e., for a chosen depth resolution, $\alpha_1$ (Equation 6) and $\alpha_2$ (Equation 7) are constant. As a consequence, $S_{\mu DHE}$ and $S_{nDHE}$ can only be reduced by minimising $S_{RSH}$ and $S_{\sigma S}$, in other words, by obtaining highly reproducible measurements of $R_{SH}$ and $\sigma_S$. One must therefore consider the importance of having reproducible measurements when performing DHE data reconstruction. Indeed, for a depth resolution of ca. 0.5 nm (as the one shown in Figure 4), targeted uncertainties of ca. 15% for $\mu_{DHE}$ and $n_{DHE}$ requires that $R_{SH}$ and $\sigma_S$ must be measured with a relative standard deviation lower than 0.1%.

Within the experimental errors discussed above, the DHE mobility profile reported in Figure 4b gives a constant value of the mobility in the first 5 nm, in perfect agreement with the uniform nature of the concentration profile. The average value obtained through the calculated DHE points (with an etching step as small as 0.5 nm) is 91.02 ± 13.08 $cm^2 \cdot V^{-1} \cdot s^{-1}$, again in agreement with the more precise value of 88.60 ± 0.27 $cm^2 \cdot V^{-1} \cdot s^{-1}$ that can be extracted from the raw mobility data (cf. Figure 3c, $r_H = 0.4$) obtained from much thicker layers (between 15 and 20 nm thick). Also, these mobility values are perfectly compatible with those predicted by analytical models for a doping concentration varying between $1 \times 10^{19}$ $cm^{-3}$ (86 $cm^2 \cdot V^{-1} \cdot s^{-1}$) and $2 \times 10^{19}$ $cm^{-3}$ (74 $cm^2 \cdot V^{-1} \cdot s^{-1}$) with $x_{Ge} = 0.23$ at $T = 300$ K according to the following expression [43]:

$$\mu_{TCAD} = \mu_{min1}\exp\left(\frac{-p_C}{N}\right) + \frac{\mu_{const} - \mu_{min2}}{1+\left(\frac{N}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1+\left(\frac{C_s}{N}\right)^{\beta}}, \quad (10)$$

with

$$\mu_{const} = \mu_{max}\left(\frac{T}{T_0}\right)^{-y}.$$

Considering the possible lack of precision in the Ge content of the layer as well as the sub-nanometric depth resolution achieved in these measurements, we can therefore conclude that the DHE method we have developed for the investigation of SiGe is consistent.

# Results and Discussion

## Study of a 6 nm boron-doped SiGeOI layer

Within the recent development of the 3D-sequential integration technology at CEA-LETI, laser annealing is being investigated as a low thermal budget solution for achieving dopant activation in the top transistor level without degrading the performance of the transistors located at the bottom [39]. The efficiency of this technique has already been proven for electrical activation of phosphorus in 22 nm thick SOI structures [44]. In this section, we extend the investigation to SiGeOI layers of 6 nm. Due to the extreme thin size of the layer and the buried oxide, classical 4PP characterization is not possible because of probe penetration down to the substrate. Thanks to Van der Pauw test structure, probe penetration has been circumvented, while conventional and differential Hall effect measurements described in the previous sections have been used to investigate dopant activation in laser-annealed ultrathin SiGeOI layers.

### Experimental details

The starting SiGeOI wafer has a SiGe top layer of 6 nm and a 20 nm thick buried oxide (BOX). The first step is the deposition of a 3nm $Si_3N_4$ directly followed by $Ge^+$ implantation to preamorphise a part of the SiGe crystal and $B^+$ implantation for p-type doping. In the following step, a second layer of 3 nm $Si_3N_4$ is deposited prior to laser thermal annealing (LTA). LTA was performed by SCREEN-LASSE using a XeCl excimer laser ($\lambda$ = 308 nm) with a pulse duration of approximately 160 ns. Finally, several 18 × 18 $mm^2$ areas where irradiated with energy densities ranging from 0.65 to 0.79 $J \cdot cm^{-2}$ (Figure S9, Supporting Information File 1).

### Structural and conventional Hall effect analysis

Prior to Hall effect analysis, we consider the structure of the layer before LTA. TEM cross-section observations (Figure S10, Supporting Information File 1) indicate that the top crystalline SiGe layer has a thickness between 5 and 6 nm, i.e., very close to the original thickness of 6 nm. Indeed, high-resolution images show that the layer thickness can rapidly vary by up to four lattice planes (i.e., ca. 1 nm) within a few nanometres. This suggests that the Ge preamorphisation implant in this wafer resulted in a damaged SiGe surface (locally amorphising it) but was not enough to produce a continuous amorphous layer.

Then, we compare electrical parameters measured by conventional Hall effect with the evolution of the crystal structure

imaged by TEM as functions of the laser energy densities. The TEM analysis (Figure S11, Supporting Information File 1) shows that for energies of 0.74 and 0.76 J/cm$^2$, the observed structure is identical to that found in the as-implanted sample with the SiGe layer being almost fully crystalline (and having a surface roughness of about 1 nm). This suggests that the laser energy density used in these cases is always lower than the threshold value necessary to melt the surface. In contrast, following a LTA at 0.79 J·cm$^{-2}$ the SiGe top layer is completely amorphous, clearly indicating that in this case the whole SiGe layer was molten, leaving no seed for a perfect recrystallization. The threshold energy for surface melt is therefore located between 0.76 and 0.79 J·cm$^{-2}$ and a rapid transition between a "no melt" and a "full melt" configuration occurs in this small energy interval.

Figure 5 reports the corresponding sheet-resistance measurements as a function of the energy densities, which illustrates two different behaviours. Below 0.74 J·cm$^{-2}$, the sheet resistance remains below 10 kΩ·sq$^{-1}$, with a slight improvement occurring when the energy density is increased (ca. 6000 Ω·sq$^{-1}$ after LTA at 0.74 J·cm$^{-2}$). This indicates that, although the laser annealing did not melt the sample surface, a non-negligible dopant activation occurs at these energies, as it will be discussed below. In contrast, a much higher sheet resistance value (ca. 55 kΩ·sq$^{-1}$) is measured in the sample annealed at 0.77 J·cm$^{-2}$. Considering that the transition between "no melt" and "full melt" of the 6 nm thick SiGe layer occurs between 0.76 and 0.79 J·cm$^{-2}$, the high sheet resistance value measured at 0.77 J·cm$^{-2}$ suggests that a "full melt" of the SiGe layer has already occurred at this energy and that most of the dopant activation is therefore lost. This behaviour is similar to that observed by Acosta Alba et al. [44] in 22 nm thick phosphorus-doped SOI, where the sudden increase in the sheet resistance values observed for high laser energies was due to the formation of a poly-Si layer as a consequence of the full melt of the entire top-Si layer during LTA.

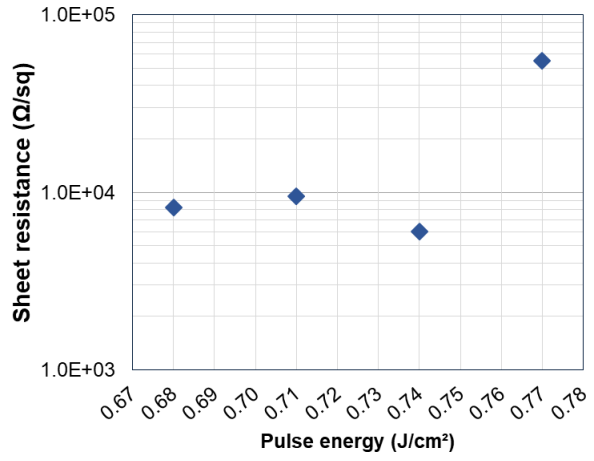



**Figure 5:** Sheet resistance as a function of the laser energy density for 6 nm SiGeOI ($x_{Ge}$ = 0.25) layer implanted with boron.

For LTA energies below the melting threshold of 0.74 J·cm$^{-2}$, some dopant activation occurs. However, the Hall effect measurements indicate that only a small fraction of the implanted boron dose is electrically active (between 6 and 12%). Two mechanisms contribute to this result: (i) the weak dopant penetration through the $Si_3N_4$ capping layer during the implantation, and (ii) the low activation rate due to the "non-melt" nature of the LTA in this energy range.

In order to investigate the first point, we calculated by using SRIM the depth distribution of the implanted boron ions according to the process conditions used in this experiment. The simulation results indicate that only about 45% of the implanted boron dose is available for electrical activation during LTA, the rest being lost in the $Si_3N_4$ capping layer or in the underlying BOX. Still, the boron dose contained in the SiGe layer after the implantation (ca. $1.8 \times 10^{14}$ cm$^{-2}$) is much higher than the electrically active dose actually measured by Hall effect ($2.3 \times 10^{13}$ cm$^{-2}$ after LTA at 0.68 or 0.71 J·cm$^{-2}$). In addition to this "dose loss" mechanism during implantation, low dopant activation must also occur during LTA.

Indeed, previous investigations [16,45] of dopant activation indicated that under similar conditions, i.e., non-amorphising implants and low thermal budget annealing (either conventional RTA or non-melt LTA), the total active dose (measured from SRP profiles) is much lower than the total implanted dose (as measured by SIMS profiles). However, the few electrically active dopant atoms present after annealing were not found to be uniformly distributed in depth but rather mostly located close to the surface, where the damage recovery, i.e., interstitial recombination is favoured (Figure S12, Supporting Information File 1). Moreover, even for the smallest thermal budgets (short RTA time or minimum number of laser shots), dopant activation at the surface was maximum or close to the solubility limit at the annealing temperature. Finally, it was found that dopant activation increases with annealing time although no dopant diffusion is detected by SIMS.

It is therefore important to verify if this behaviour also occurs in the case of ultrathin laser-annealed SiGeOI samples. Indeed, within the application of laser annealing in strategies to reduce contact resistance, such a result may constitute a big step forward. One of the LTA samples investigated in this work has therefore been analysed by the differential Hall effect technique, and results are presented in the next section.

## Differential Hall effect analysis

The SiGeOI sample implanted with boron and annealed with an energy density of 0.68 J·cm$^{-2}$ was used for these investigations. Four successive SC1 etching processes have been performed for a total etching time of 30, 50, 70 and 90 min, reducing, respectively, the total thickness by 0.1, 0.3, 0.8 and 1.3 nm (confirmed by ellipsometry measurements and TEM images). Concerning surface roughness, TEM images dos not show significant surface roughness, indicating that the surface quality is not degraded by the etch process. This was confirmed by AFM analysis on 500 × 500 nm$^2$ areas taken from the Van der Pauw sample used for the Hall effect measurements after the longest etch process (90 min; Figure S13, Supporting Information File 1). Compared to the non-etched region (average roughness of 0.18 nm), the surface roughness is slightly higher in the etched regions (between 0.26 and 0.34 nm) but always much smaller than the total etched thickness (1.3 nm in this sample). Considering that these measurements were performed after the longest etch process and that the surface roughness increases with etching time, we can conclude that the surface roughness induced by the etch process is always negligible and is not expected to have any impact on the reliability of the Hall effect measurements.

The results of the Hall effect measurements (raw data $R_S$, $N_H$ and $\mu_H$) performed before etch and after each removal step are reported in Figure 6 as functions of the removed thickness. It appears that the sheet resistance $R_S$ increases very rapidly after each step, with the $R_S$ values increasing by a factor of four between the second and the third etch step. In fact, only the points corresponding to the three first etch steps are reported in the figure. Following the fourth and longest etch process (1.3 nm removed thickness) the sample was so resistive that quantitative values could not be measured. Correspondingly, the Hall dose $N_H$ is found to rapidly decrease as the etching progresses, qualitatively indicating that most of the active dose is located close to the surface.

Following the differential Hall data treatment method discussed in the previous sections, the depth distributions of the active dopant concentration and of the carrier mobility have finally been extracted and are reported in Figure 7. The data quantita-

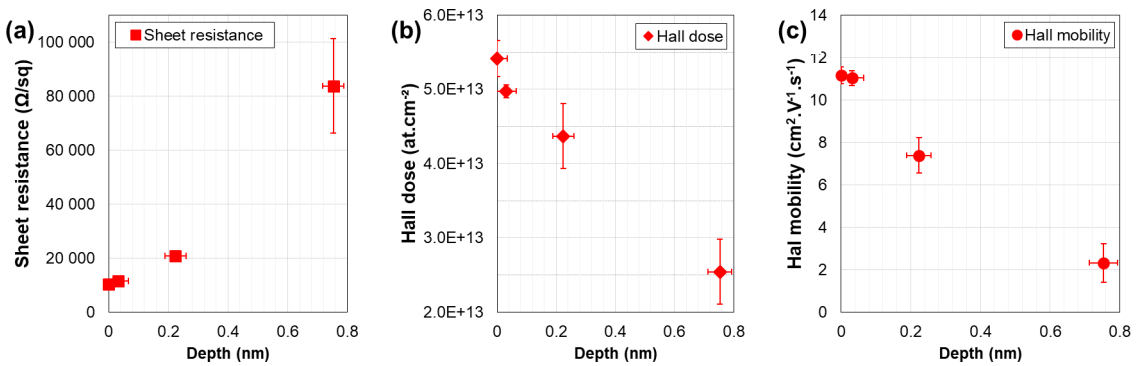



**Figure 6:** Hall effect measurements (raw data: (a) $R_S$, (b) $N_H$ and (c) $\mu_H$) of the SiGeOI sample ($x_{Ge}$ = 0.25) implanted with boron and annealed at an energy of 0.68 J·cm$^{-2}$ as a function of the etched thickness (as measured by ellipsometry).

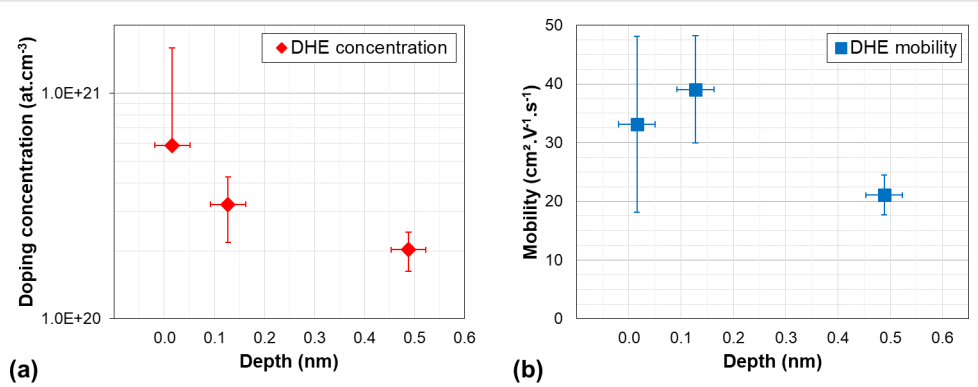



**Figure 7:** Depth profiles of (a) active dopant concentration and (b) carrier mobility extracted from DHE measurements of a SiGeOI sample ($x_{Ge}$ = 0.25) implanted with boron and annealed at an energy of 0.68 J·cm$^{-2}$.

tively confirm the results suggested by the Hall effect raw data: The active dopant concentration is highest at the surface with a value as high as ca. $6 \times 10^{20}$ cm$^{-3}$ and it rapidly decreases within the first nanometres below the surface ($2 \times 10^{20}$ cm$^{-3}$ at 0.8 nm). Corrections of the depth scale related due to the surface-depletion effect have been neglected due to high doping level measured in this sample (cf. previous section) unless we give a numerical value.

This result is in agreement with the scenario discussed in the previous section. Indeed, due to the "non-melt" nature of the annealing, and considering that no amorphisation of the surface was achieved during the implantation, the extremely low thermal budget provided by the LTA process is not efficient in removing the implant damage in the material, except in the surface region where interstitial recombination (and hence damage recovery) occurs. As a consequence, below the surface, not only the active dopant concentration is much lower than at the surface, but also the residual damage is extremely high, which is expected to have an impact on the carrier mobility. This is clearly confirmed by the Hall mobility (Figure 7b) the value of which at a depth of 0.8 nm below the surface (ca. 20 cm$^2$·V$^{-1}$·s$^{-1}$) is much lower than the carrier mobility at the surface (ca. 35 cm$^2$·V$^{-1}$·s$^{-1}$), in spite of a much lower carrier concentration. Alternative mechanisms as the reasons for this mobility reduction below the surface can be excluded, including surface roughness (Figure S13, Supporting Information File 1), and surface depletion due to interface states (cf. previous sections).

In any case, although the investigated doping process is at a preliminary stage, the detailed investigation carried out in this work allows us to conclude that a doping process based on nanosecond-laser annealing can be successfully applied to ultrathin SiGeOI layers of about 6 nm thickness, while obtaining active dopant concentrations at the surface well above $1 \times 10^{20}$ cm$^{-3}$. This is a promising result in view of improving contact resistivity in source/drain regions of advanced devices.

## Study of 11 nm arsenic-doped SOI layer

In the perspective of improving the contact resistance within FDSOI technology [6], different annealing methods are investigated for the increase of dopant activation close to the surface. In this section we will focus on the comparison between conventional spike-RTA and millisecond-laser dynamic surface annealing (DSA), both applied to 11 nm thick n-type doped SOI layers. In addition to SIMS, TEM and conventional Hall effect measurements, differential Hall profiling will be shown to allow a reliable estimation of the dopant activation level within the first nanometres below the silicon surface.

### Experimental details

Two 11 nm thick SOI wafers were used for this experiment (BOX thickness: 25 nm, as confirmed by ellipsometry). The wafers were implanted with 3 keV As$^+$ ions to a dose of $1 \times 10^{14}$ cm$^{-2}$. The implantations were performed through a thin thermal oxide layer (ca. 1 nm thick) grown on the as-received wafers. Following the implantations, each wafer underwent a different annealing process: 1050 °C spike-RTA in $O_2/N_2$ atmosphere in one case, 0.3 ms laser-DSA in $N_2$ atmosphere in the other case.

### Chemical profiles and conventional Hall effect measurements

SIMS characterisations were carried out after annealing in both samples without stripping the thermal oxide. The results are shown in Figure 8 for both arsenic (Figure 8a) and oxygen (Figure 8b). The As concentration profile of the RTA-annealed wafer exhibits a peak value of ca. $3 \times 10^{20}$ cm$^{-3}$ just below the surface, followed by a quasi-plateau ($6–7 \times 10^{19}$ cm$^{-3}$) in the

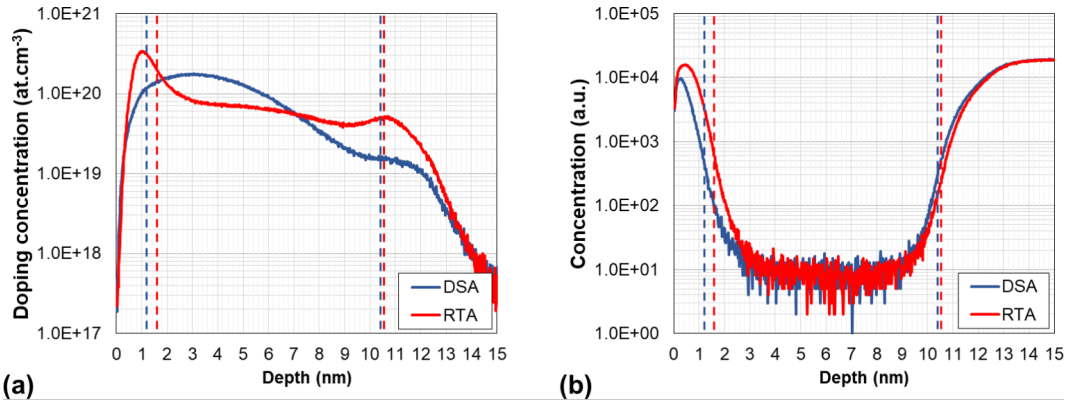



**Figure 8:** Concentration depth profiles of (a) arsenic and (b) oxygen measured by SIMS in 11 nm thick SOI wafers implanted with arsenic and annealed by RTA (red curves) or DSA (blue curves).

rest of the Si top layer. In contrast, the As profile of the DSA wafer is closer to a Gaussian shape, with a peak concentration of about $2 \times 10^{20}$ cm$^{-3}$ at a depth of ca. 3 nm. In both cases, the sharp decrease of the As concentration below 11 nm corresponds to the transition from the Si top layer to the buried oxide. Similarly, the As signal in the first nanometres below the surface originates from the dopant atoms contained in the thermal oxide formed prior to the implantation. It is therefore critically important to localise the actual position of the oxide/top Si interface in view of the reliable interpretation of the Hall effect data in terms of dopant activation efficiency, i.e., estimation of the active dopant fraction. To this purpose, we used the oxygen SIMS concentration profiles (Figure 8b) to estimate the position of the oxide/top Si and of the top Si/BOX interfaces in correspondence of the maximum slope of the oxygen signal. The position of the $SiO_2$/Si interfaces determined in this way (1.2 nm and 1.6 nm below the surface for the DSA- and RTA-annealed wafers, respectively) are in perfect agreement with those found by STEM-EDX measurements carried out using an aberration-corrected TEM instrument (see Figure S14, Supporting Information File 1, for the RTA-annealed wafer) and are reported as dashed lines in Figure 8.

Conventional Hall effect measurements were performed on both annealed wafers and are reported in Table 1 (a scattering factor $r_H = 1$ was chosen in this case [20]). The results indicate that both annealing treatments yield high dopant activation, with millisecond-DSA resulting in slightly better parameters, i.e., a higher active dopant density and an overall lower sheet resistance compared to spike-RTA. Indeed, using the analysis method described in [13] and taking into account the exact location of the $SiO_2$Si interfaces (as described above), we found that about 92% of the arsenic ions retained in the top Si layer are electrically active in the DSA-annealed wafer, with a maximum active concentration of ca. $1.4 \times 10^{20}$ cm$^{-3}$, compared to about 75% and ca. $6 \times 10^{19}$ cm$^{-3}$, respectively, in the RTA-annealed wafer. However, these average values do not give access to the actual dopant concentration levels in the surface region. DHE profiling was therefore used to scan the surface doping concentration in both investigated wafers.

**Table 1:** Hall effect data measured on 11 nm thick SOI wafers implanted with $As^+$ (3 keV, $1 \times 10^{14}$ cm$^{-3}$) and annealed with spike-RTA or millisecond-laser-DSA.

| annealing treatment | sheet resistance, $R_S$ ($\Omega \cdot sq^{-1}$) | active Hall dose, $N_H$ ($cm^{-2}$) | Hall mobility, $\mu_H$ ($cm^2 \cdot V^{-1} \cdot s^{-1}$) |
|---|---|---|---|
| RTA | 2157 | $4.5 \times 10^{13}$ | 65 |
| DSA | 1643 | $7.8 \times 10^{13}$ | 49 |

## Differential Hall effect

For these measurements, after each removal step (based on HF/ethanol cycle) the Van der Pauw test structures were left in a clean-room environment from one to three days, so to provide reproducible native oxide regrowth. In order to collect a maximum number of data, we performed thickness and Hall effect measurements before and after oxide stripping. However, considering the possible difference in the electrostatic configuration of the surface, i.e., the number of interface states, between samples with a stable grown oxide and samples measured just after stripping of the native oxide, and the impact of the electrostatics on the reproducibility of the Hall effect measurements (cf. Figure 4a and the related discussion), the DHE data treatment was applied separately to the two sample groups: those measured just after oxide stripping and those measured in the presence of a stable native oxide.

Four successive etching processes were realised for each sample resulting in eight experimental points. All the raw Hall data from both investigated samples are reported in Figure 9. When the layer thickness decreases, the electrical parameters evolve

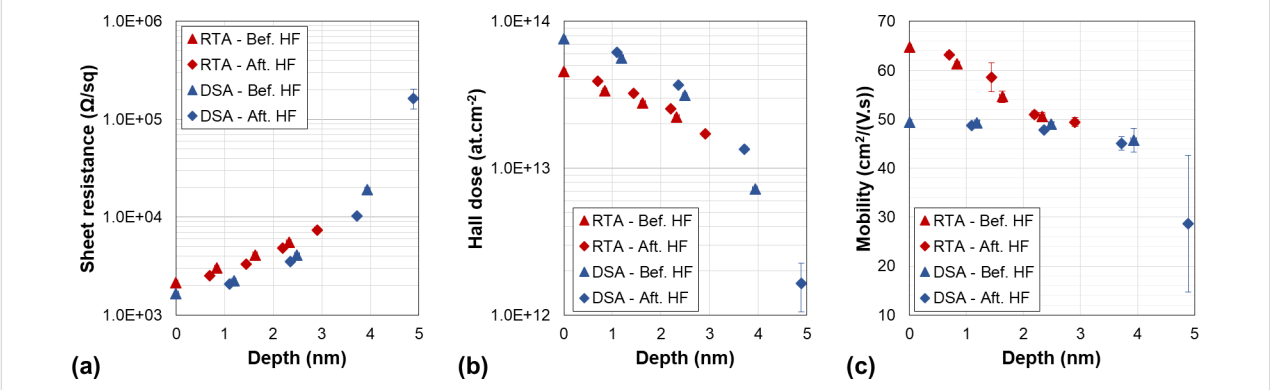



**Figure 9:** Hall effect measurements (raw data: (a) $R_S$, (b) $N_H$ and (c) $\mu_H$) of the SOI samples implanted with arsenic and annealed with DSA (red symbols) and RTA at 1050 °C (blue symbols), as a function of the etched thickness (as measured by ellipsometry).

following the expected behaviour, with the sheet resistance increasing and the active Hall dose decreasing as a function of the removed thickness. However, due to non-uniformity of the dopant distribution in depth, the observed variations are not linear. As for the carrier mobility, the RTA-annealed samples exhibits higher values than the DSA-annealed samples, in agreement with the lower active dopant concentration already inferred from conventional Hall measurements (cf. Table 1).

In addition, it has to be noted that the samples could not be profiled over the entire thickness of the active layer, as indicated by the unexpectedly high resistance value of the DSA annealed sample after 5 nm of etching (Figure 9a), and in apparent contrast with the high active fraction (>90%) of this sample (Table 1). This is attributed to the presence of the backside depletion region located at the Si/BOX interface, the impact of which on the measured values increases with the increase of the removed thickness. As reported in previous studies in similar SOI structures [18], this effect does not modify the reliability of the dopant concentration extracted at the surface, where it exhibits its maximum value. A possible solution to overcome this problem could consist in the local modification of the dopant concentration at the Si/BOX interface (for instance by a dedicated low-dose implant) so to strongly reduce the extent of the backside depletion region. However, such additional step was not considered in this work, the main focus of which is on the dopant activation at the semiconductor surface.

The calculated differential Hall values are finally presented in Figure 10. The obtained values are plotted together with arsenic concentration profiles measured by SIMS, by taking into account the actual position of the $SiO_2$/top Si interface (cf. Figure 8), while corrections of the depth scale related due to the surface depletion effect have been neglected due to high doping levels measured in these samples (cf. previous section and Figure S7, Supporting Information File 1). The DHE carrier concentration profiles perfectly follow the chemical profiles measured by SIMS, confirming that both annealing methods provide a high dopant activation efficiency. More importantly, DHE measurements unambiguously show that, within the first two nanometres below the surface, millisecond annealing results in a higher active dopant concentration compared to RTA, making DSA a better candidate than RTA for contact resistance reduction in future FDSOI technologies.

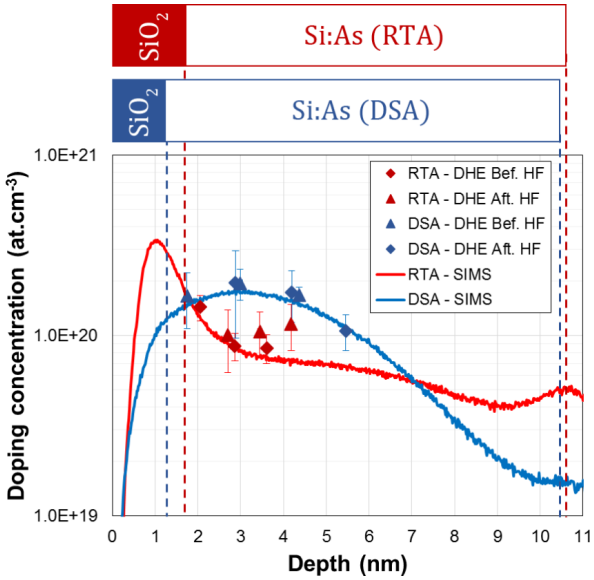



**Figure 10:** Active dopant concentration depth profiles as extracted by DHE measurements from 11 nm thick SOI wafers implanted with $As^+$ (3 keV, 1 × $10^{14}$ $cm^{-3}$) and annealed with spike-RTA (red symbols) or millisecond-laser-DSA (blue symbols). DHE values are compared with the corresponding arsenic chemical concentration profiles as measured by SIMS.

## Conclusion

In this paper, we presented an enhanced differential Hall effect measurement method that allows to determine, with sub-nanometre resolution, the level of dopant activation close to the surface for Si and SiGe. In the case of SiGe, which constitutes the most challenging process, we showed the reliability of the SC1 chemical solution thanks to its slow etch rate, stoichiometry conservation and low roughness generation. For both materials, our method include a direct measurement of the removed thickness after each removal step, so to avoid averaging the etch rate and improve the accuracy of calculated values. Then, we demonstrated the reliability of a complete DHE procedure, with an etching step as small as 0.5 nm, on a dedicated 20 nm thick SiGe test structure fabricated by CVD and uniformly doped in situ with boron during growth.

The developed method was finally applied to the investigation of dopant activation achieved by advanced annealing methods in two material systems: 6 nm thick SiGeOI and 11 nm thick SOI. In the first case, we showed that a doping process based on nanosecond-laser annealing can be successfully applied to ultra-thin SiGeOI layers, with achieved active dopant concentrations at the surface well above 1 × $10^{20}$ $cm^{-3}$, which is a promising result in view of improving contact resistivity in SiGe source/drain regions of advanced devices. In the second case, DHE measurements unambiguously show that, within the first few nanometres below the surface, millisecond-laser-DSA can result in a higher active dopant concentration compared to RTA, making DSA a better candidate than RTA for contact resistance reduction in future FDSOI technologies. In summary, thanks to the improvements implemented in this work, DHE is shown to be a unique sensitive characterisation technique for a detailed

investigation of dopant activation in ultrashallow layers, providing sub-nanometre resolution for depth profiles of both dopant concentration and carrier mobility.

## Supporting Information

### Supporting Information File 1

Additional experimental data.
[https://www.beilstein-journals.org/bjnano/content/supplementary/2190-4286-9-184-S1.pdf]

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# A variable probe pitch micro-Hall effect method

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## Abstract

Hall effect metrology is important for a detailed characterization of the electronic properties of new materials for nanoscale electronics. The micro-Hall effect (MHE) method, based on micro four-point probes, enables a fast characterization of ultrathin films with minimal sample preparation. Here, we study in detail how the analysis of raw measurement data affects the accuracy of extracted key sample parameters, i.e., how the standard deviation on sheet resistance, carrier mobility and Hall sheet carrier density is affected by the data analysis used. We compare two methods, based primarily on either the sheet resistance signals or the Hall resistance signals, by theoretically analysing the effects of electrode position errors and electrical noise on the standard deviations. We verify the findings with a set of experimental data measured on an ultrashallow junction silicon sample. We find that in presence of significant electrical noise, lower standard deviation is always obtained when the geometrical analysis is based on the sheet resistance signals. The situation is more complicated when electrode position errors are dominant; in that case, the better method depends on the experimental conditions, i.e., the distance between the insulating boundary and the electrodes. Improvement to the accuracy of Hall Effect measurement results is crucial for nanoscale metrology, since surface scattering often leads to low carrier mobility.

## Introduction

Materials characterization becomes increasingly difficult as the dimensions of transistors continue to decrease. Although three dimensional electrical characterization is the ultimate goal of materials characterization, conventional metrology for thin-film characterization still plays an important role in development of materials used in nanoelectronics [1]. Hall effect measurements have been employed for decades to electrically characterize samples and extract important metrics, such as concentration, mobility and type of charge carriers [2,3]. Some of the measurement methods require significant sample preparation while other methods are destructive [2]. Great progress in measurement simplicity and accuracy has been achieved with the intro-

duction of the micro-Hall effect (MHE) method [4]. The MHE measurement itself is performed simply by placing a micro four-point probe (M4PP) in parallel and close proximity to an insulating boundary, with an orthogonal magnetic field applied. Then the measured resistance will have three contributions: a drift term, a Hall effect term and a magnetoresitive term. In a comparative study by Clarysse et al., the MHE method has been shown to have higher accuracy than more conventional setups using square van der Pauw geometries [5]. Van der Pauw geometries often suffer from inaccurate contact placement, which easily results in measurement errors of a few percent [6]. Comparing the MHE method with measurements performed using a cloverleaf, Petersen et al. [7] have shown a 1:1 correlation between the measurements. Cloverleaf measurements are, however, challenging because of the sample definition required before any actual measurements can be performed. Hence, the MHE method holds several advantages over other well-known techniques, even though low-mobility samples can also be characterized by the latter [8].

The key to accurate extraction of sheet resistance $R_0$, Hall sheet carrier density $N_{HS}$ and Hall mobility $\mu_H$ from MHE measurements is to determine the exact distance between the probe and the insulating boundary. To this end, different measurement strategies have been described using micro four-point probes [4,9-11]. Most recently, a strategy based on variable probe pitch measurements using a multi-point probe with different subsets of four electrodes has been developed [11,12]. Similar strategies using variable probe pitch multi-point probes have been used for other systems, including current-in-plane tunneling measurements [13], junction-leakage measurements [14] and surface-conductivity measurements of bulk materials [15,16].

In this study, we present the variable probe pitch MHE method applied to an equidistant micro seven-point probe (M7PP), and compare two independent ways of extracting the relevant sample parameters from the same set of measurements. Furthermore, we will demonstrate the sensitivity of each method to position errors, as well as to electrical noise. Finally, we will present measurements on a B-doped Si ultrashallow junction, supporting our findings.

## Micro-Hall Effect Theory

The fundamentals of Hall Effect measurements with a collinear M4PP have previously been described in detail [4]. However, we will briefly outline some of the most important characteristics here. For any four-point probe, 6 non-trivial configurations of current and electrode pins can be measured, but for this work, only the configuration pairs (A, A') and (B, B'), illustrated in Figure 1, are relevant.

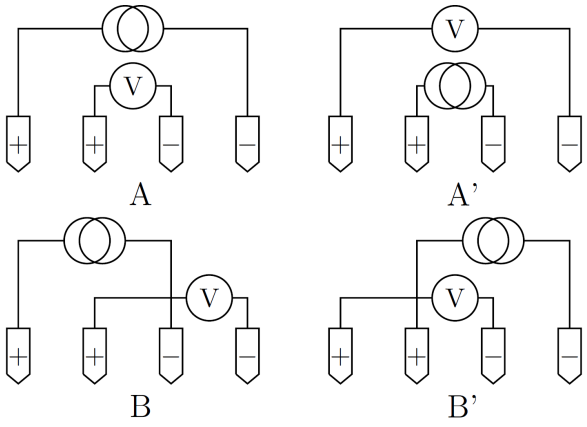



**Figure 1:** The standard probe pin configurations A, A', B and B' used in the experiments.

Crucial in understanding MHE measurements are the definitions of the resistance difference for the pairs, $\Delta R_{XX'} \equiv R_X - R_{X'}$, as well as their resistance average, $\overline{R_{XX'}} \equiv (R_X + R_{X'})/2$, where $X \in \{A,B\}$. For an equidistant four-point probe placed parallel to an insulating boundary, the resistance difference for the (B, B') pair is

$$\Delta R_{BB'} = \frac{2R_H}{\pi}\left(3\arctan\frac{s}{2y_0} - \arctan\frac{3s}{2y_0}\right), \tag{1}$$

where $R_H$ is the Hall sheet resistance, $s$ is the electrode pitch and $y_0$ the distance between the probe and the insulating boundary. Note that in the relevant case where the probe is placed parallel to a straight insulating boundary, the resistance difference for the (A, A') pair is $\Delta R_{AA'} = 0$. The resistance averages in the configuration pairs (A, A') and (B, B') are

$$\overline{R_{AA'}} = \mathcal{A}_+ \ln 4 + \mathcal{A}_- \ln\frac{4+4\left(y_0/s\right)^2}{1+4\left(y_0/s\right)^2}, \tag{2}$$

$$\overline{R_{BB'}} = \mathcal{A}_+ \ln 3 + \mathcal{A}_- \ln\sqrt{\frac{9+4\left(y_0/s\right)^2}{1+4\left(y_0/s\right)^2}}, \tag{3}$$

respectively, where the coefficients are given by

$$\begin{aligned} A_+ &\equiv \frac{R_0}{2\pi}\left(1+\frac{R_H^2}{R_0^2}\right), \\ A_- &\equiv \frac{R_0}{2\pi}\left(1-\frac{R_H^2}{R_0^2}\right), \end{aligned} \tag{4}$$

in which $R_0$ denotes the sheet resistance. It has been shown that by introducing a pseudo sheet resistance $R_p$, the effect of electrode position errors can be mitigated [9]. The pseudo sheet resistance is defined as the solution to the modified van der Pauw equation [17-20]

$$\exp\frac{2\pi\overline{R_{AA'}}}{R_p}-\exp\frac{2\pi\overline{R_{BB'}}}{R_p}=1, \tag{5}$$

which will be utilized in the next section, in which the variable probe pitch method is presented in full.

## Variable Probe Pitch Method

The variable probe pitch method uses measurements at different relative distances to the boundary of a sample by multiplexing several sets of four electrodes on a M7PP. These sets are called sub-probes and can be chosen with different electrode pitch. In this case, three equidistant sub-probes are used and named with reference to the index number of the four electrodes constituting the sub-probe, "1357" (20 µm pitch), "1234" and "4567" (10 µm pitch). The three sub-probes are outlined in Figure 2. Once resistance measurements have been performed in the A, A', B and B' configurations for the three sub-probes, two different ways of determining the distance to the boundary and ultimately obtaining the desired parameters, can be employed. The first method utilizes the Hall signal and will be referred to as the "Hall signal method". The second method uses the resistance signal and will be referred to as the "resistance signal method".

To determine the distance to the boundary, $y_0$, the first step in the Hall signal method is to exploit the fact that the Hall signal decreases with distance to the boundary relative to the probe pitch, as shown in Figure 3. In other words, it is possible to uniquely determine $y_0$ by taking the ratio of two Hall signals ($\langle\Delta R_{BB'1}\rangle$ and $\Delta R_{BB'2}$) measured while using sub-probes with different pitches $s_1$ and $s_2$, i.e., by using the Hall signal $\Delta R_{BB'2}$ from the large probe, 1357, and the average of the Hall signals $\langle\Delta R_{BB'1}\rangle$ from the smaller probes, 1234 and 4567,

$$\frac{\Delta R_{BB'2}}{\langle\Delta R_{BB'1}\rangle}=\frac{f\left(y_0/s_2\right)}{f\left(y_0/s_1\right)}, \tag{6}$$

where f(·) is a geometrical function obtained from Equation 1.

To calculate $y_0$ in the resistance signal method, dual-configuration position correction is utilized, by inserting the measured

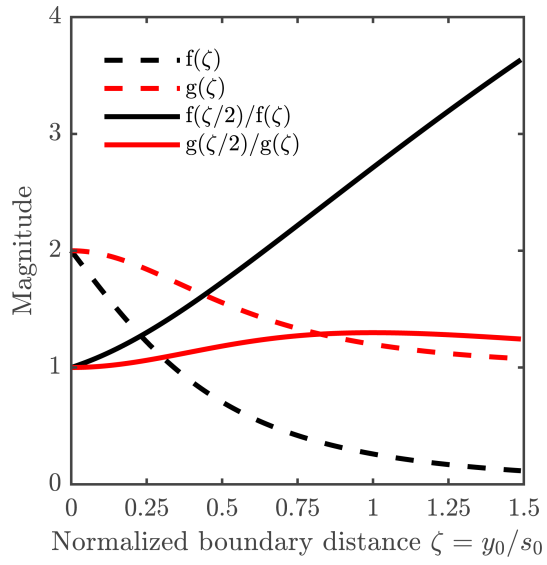



**Figure 3:** The dashed curves show the relative Hall signal $\Delta R_{BB'}/R_H$ = f(ζ) (Equation 1) and relative pseudo sheet resistance $R_P/R_0$ = g(ζ) (Equation 5), as a function of normalized distance to the boundary ζ = $y_0/s_0$. The full curves show the ratios used in the Hall signal method $\Delta R_{BB'2}/\Delta R_{BB'1}$ = f(ζ/2)/f(ζ) and the resistance signal method $R_{P2}/\Delta R_{P1}$ = g(ζ/2)/g(ζ), respectively, as a function of the normalized boundary distance.

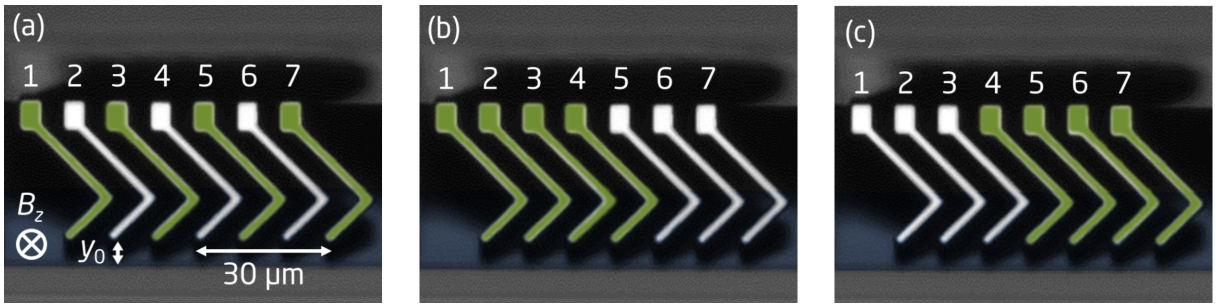



**Figure 2:** The three sub-probes on an M7PP used for multiplexing during measurements; a) 1357 (20 µm pitch), b) 1234 and c) 4567 (10 µm pitch). The electrode pins used in a given sub-probe are marked with green. The sample itself is highlighted in blue. The direction of magnetic flux density $B_z$, which is pointing into the sample, is also indicated.

resistance averages for each sub-probe in the van der Pauw equation (Equation 5). From this equation, the pseudo sheet resistance is extracted, which, due to the presence of the boundary, differs from the true sheet resistance, $R_0$. By measuring the pseudo sheet resistances, $\langle R_{P1}\rangle$ and $R_{P2}$, at different relative distances to the boundary, using differently pitched ($s_1$, $s_2$) sub-probes, i.e., by using the resistance signal $R_{P2}$ from the large probe, 1357, and the average of the resistance signals $\langle R_{P1}\rangle$ from the smaller probes, 1234 and 4567, it is possible to determine $y_0$ from

$$\frac{R_{P2}}{\langle R_{P1}\rangle} = \frac{g(y_0/s_2)}{g(y_0/s_1)}, \tag{7}$$

where g(·) is a geometrical function, implicitly found from Equation 2, Equation 3 and Equation 5.

Equation 6 and Equation 7 are plotted in Figure 3 for the specific case of a probe having the reference pitch $s_0$ for the two smallest sub-probes and $2s_0$ for the larger sub-probe. They are plotted as a function of the normalized boundary distance $\zeta = y_0/s_0$. We introduce $s_0$ and $\zeta$ here to emphasize the nature and relationship between the sub-probes used in this paper; the pitches $s_1$ and $s_2$ utilized in this section are more general in nature and could also be used to describe other symmetric multipoint-probes.

After $y_0$ has been calculated using either method, the Hall sheet resistance $R_H$ and the sheet resistance $R_0$ can be determined by means of

$$R_H = \Delta R_{BB'i}/f(y_0/s_i), \tag{8}$$

$$R_0 = R_{Pi}/g(y_0/s_i), \tag{9}$$

respectively, with $i \in [1,2]$. Finally, the Hall sheet carrier density, $N_{HS}$, and the Hall mobility, $\mu_H$, can be found from [4]

$$N_{HS} = \frac{B_z}{ZeR_H}, \tag{10}$$

and

$$\mu_H = \frac{ZR_H}{R_0 B_z}, \tag{11}$$

where $Z$ is the sign of the charge carrier and $e$ is the elementary charge.

The choice of using seven equidistant electrodes for the probe was carefully made, in order to minimize the contribution of in-line geometrical errors to the measured quantities, $\Delta R_{BB'}$ and $R_P$. The definitions of in-line and off-line geometrical errors of an M7PP are illustrated in Figure 4. Any in-line errors on pins 1 and 7 will influence the size of the large sub-probe and the average size of the small sub-probes, which explains the correlation between values measured with sub-probe 1357, and the average values obtained with sub-probes 1234 and 4567. Furthermore, an in-line error on pin 4 would be inconsequential, as the pin is shared by the two 10 µm sub-probes. Such an error will cause an increase in the measured quantity of one sub-probe, whereas a decrease in the measured quantity will result from the other, leaving the average value unchanged. Hence, it should be possible to eliminate the correlated in-line errors on pins 1, 4 and 7, while in-line errors on pins 2, 3, 5 and 6 have low or zero influence on the measured quantities $R_p$ and $\Delta R_{BB'}$. Off-line position errors can result in complex errors that are correlated to some extent, but these are beyond the scope of this study. Electrical noise will produce uncorrelated errors on the measurements, which cannot be corrected.

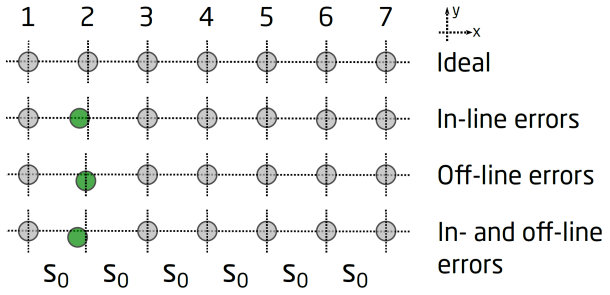



**Figure 4:** Static position errors: at the top, the ideal positions of a M7PP is shown. Below, the case of only in-line errors of the same probe can be seen, the affected pin marked with green (position error in the *x*-direction). Next, the case of only off-line errors is outlined using the same pin (position error in the *y*-direction) and at the bottom, a combination of in- and off-line errors on one of the pins is sketched.

The sensitivity of the resistance signal method and the Hall signal method to position errors, as well as electrical noise, will be studied in the next section, to investigate which of the two independent methods perform best, and under which circumstances.

## Results and Discussion

In this section, we will evaluate numerically the expected measurement precision of the Hall signal method and the resistance signal method. The two main sources of error are geometrical errors and electrical noise, which we initially will discuss separately.

In the evaluation of geometrical errors, we will only consider mutually independent and normally distributed static position errors, meaning that if a position error is present on one of the electrode pins, this error will not change during a measurement. The relative standard deviation due to position errors, $\sigma_\beta^{\mathrm{rel,pos}}$, for a given property $\beta \in \{R_0, \mu_H, N_{HS}\}$ can be calculated from

$$\begin{aligned}\sigma_\beta^{\mathrm{rel,pos}} &= \frac{1}{\beta}\sqrt{\sum_{n=1}^{7}\left[\left(\frac{\partial\beta}{\partial x_n}\sigma_x\right)^2+\left(\frac{\partial\beta}{\partial y_n}\sigma_y\right)^2\right]} \\ &\simeq \sqrt{\sum_{n=1}^{7}\left[\left(\frac{s_0}{\beta}\frac{\partial\beta}{\partial x_n}\right)^2+\left(\frac{s_0}{\beta}\frac{\partial\beta}{\partial y_n}\right)^2\right]}\cdot\frac{\sigma_{\mathrm{pos}}}{s_0} \\ &= \mathcal{S}_\beta^{\mathrm{pos}}\frac{\sigma_{\mathrm{pos}}}{s_0},\end{aligned} \tag{12}$$

where we have normalized to the reference pitch $s_0$. The standard deviations of in-line and off-line electrode position errors are assumed to be identical, $\sigma_{pos} = \sigma_x = \sigma_y$. The symbols $x_n$ and $y_n$ are the $x$- and $y$-positions, respectively, of the $n$-th electrode pin. $\mathcal{S}_\beta^{\mathrm{pos}}$ is the effective sensitivity of a given parameter to the relative position errors. This effective sensitivity is evaluated numerically for each parameter β and plotted in Figure 5, for both methods. The results generally predict an increased error with increasing distance from the boundary. The largest error is found for $N_{HS}$ and the lowest for $R_0$. Interestingly, the error of $\mu_H$ is lower than that of $N_{HS}$, indicating a correlation of the errors of $R_0$ and $R_H$. This effect has previously been observed experimentally [9]. For the sheet resistance, the resistance signal method has the lowest relative standard deviation up to a distance of $y_0 = 0.53s_0$ away from the boundary, beyond which point a higher precision can be obtained using the Hall signal method. The same tendencies are displayed for the Hall mobility and the Hall sheet carrier density for which the method of highest accuracy changes at $y_0 = 0.41s_0$ and $y_0 = 0.45s_0$, respectively. The superiority of the resistance signal method closer to the boundary stems from the high precision on the pseudo sheet resistance ratio (Equation 7). For longer boundary distances, the pseudo sheet resistance ratio ceases to increase with boundary distance and finally starts declining as shown in Figure 3 and thus this ratio becomes less accurate for determining the boundary distance at larger distances. Since the resistance difference ratio (Equation 6) continues to increase with boundary distance, it becomes more suitable for determining the boundary distance and subsequently $R_0$, $N_{HS}$ and $\mu_H$ at larger boundary distances. Figure 3 also shows that the resistance signal method does not result in a unique solution for the boundary distance at larger boundary distances. Thus, it is necessary to place the probe within a distance of approximately $y_0 < s_0$ from the boundary.

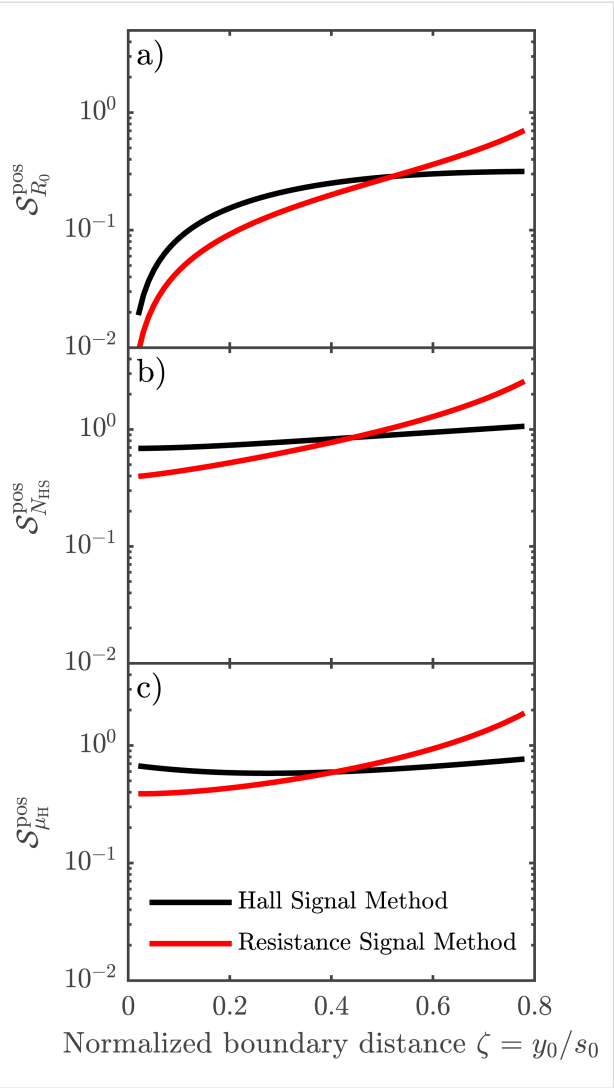



**Figure 5:** Effective sensitivity $\mathcal{S}_\beta^{\mathrm{pos}}$ for a) $R_0$, b) $N_{HS}$ and c) $\mu_H$ when in- and off-line errors are present during the measurements. The resistance signal method results in the lowest sensitivities close to the edge, whereas the Hall signal method provides better results farther away from the boundary.

To evaluate the contribution of electrical noise to MHE measurements, we consider twelve resistance measurements ($R_m$, $m \in [1,2\ldots12]$), i.e., four configurations for each sub-probe, in which a random voltage noise is present. The voltage noise comprises, e.g., Johnson noise from the two-point resistance and wiring resistance, as well as noise from the measurement electronics. The voltage noise is assumed to have the same standard deviation $\sigma_v = 60$ nV for all twelve resistance measurements [21], which in turn are assumed to be uncorrelated. The voltage noise causes a noise in the resistance measurements with the standard deviation $\sigma_{R_m} = \sigma_v / I$, where $I$ is the measurement current. From the twelve configurations measured, the parameter β is calculated, and thus the relative standard deviation on β due to electrical noise is

$$\sigma_{\beta}^{\mathrm{rel,el}} = \frac{1}{\beta}\sqrt{\sum_{m=1}^{12}\left(\frac{\partial\beta}{\partial R_m}\sigma_{R_m}\right)^2} = \sqrt{\sum_{m=1}^{12}\left(\frac{R_0}{\beta}\frac{\partial\beta}{\partial R_m}\right)^2}\cdot\frac{\sigma_v}{IR_0} = \mathcal{S}_{\beta}^{\mathrm{el}}\frac{\sigma_v}{IR_0}, \tag{13}$$

where $\mathcal{S}_{\beta}^{\mathrm{el}}$ is a dimensionless sensitivity of β to electrical noise. This effective sensitivity has been calculated numerically for the sheet resistance, Hall mobility and Hall sheet carrier density, while choosing the ratio $R_H/R_0$ = 3:1000 to represent the experiments, and the ratio $R_H/R_0$ = 1:100 for comparison. These results are shown in Figure 6a–c and Figure 6d–f, respectively, for both methods. There are two main mechanisms describing the results shown in Figure 6: (1) the accuracy with which the distance to the boundary is determined and (2) how the position uncertainty translates into an error in the calculation of $R_H$ and $R_0$.

Figure 7 generalizes the results from Figure 6 in the sense that the sensitivity of each parameter to electrical noise is investigated for varying $R_H/R_0$ ratios. A small $R_H/R_0$ ratio corresponds to a low mobility sample or a setup using a small magnetic field, whereas a higher ratio indicates the opposite. We have chosen to investigate $R_H/R_0$ ratios from $3 \times 10^{-3}$ to $1 \times 10^{-1}$, because of the nature of Equation 13, which takes into account only errors of first order. Investigating $R_H/R_0$ ratios below $3 \times 10^{-3}$ would produce cases where the electrical noise we apply is comparable to or greater than the Hall signal, in which case Equation 13 is no longer valid. The probe is placed at a distance of $y_0 = 0.4s_0$ away from the insulating boundary, as it is most commonly done in experiments. Consider then the parameters $R_0$, $\mu_H$ and $N_{HS}$, as produced by the Hall signal method, and outlined in Figure 7a–c using black lines. In all three cases, we observe a similar relative decrease of $\mathcal{S}_{\beta}^{\mathrm{el}}$ with increasing

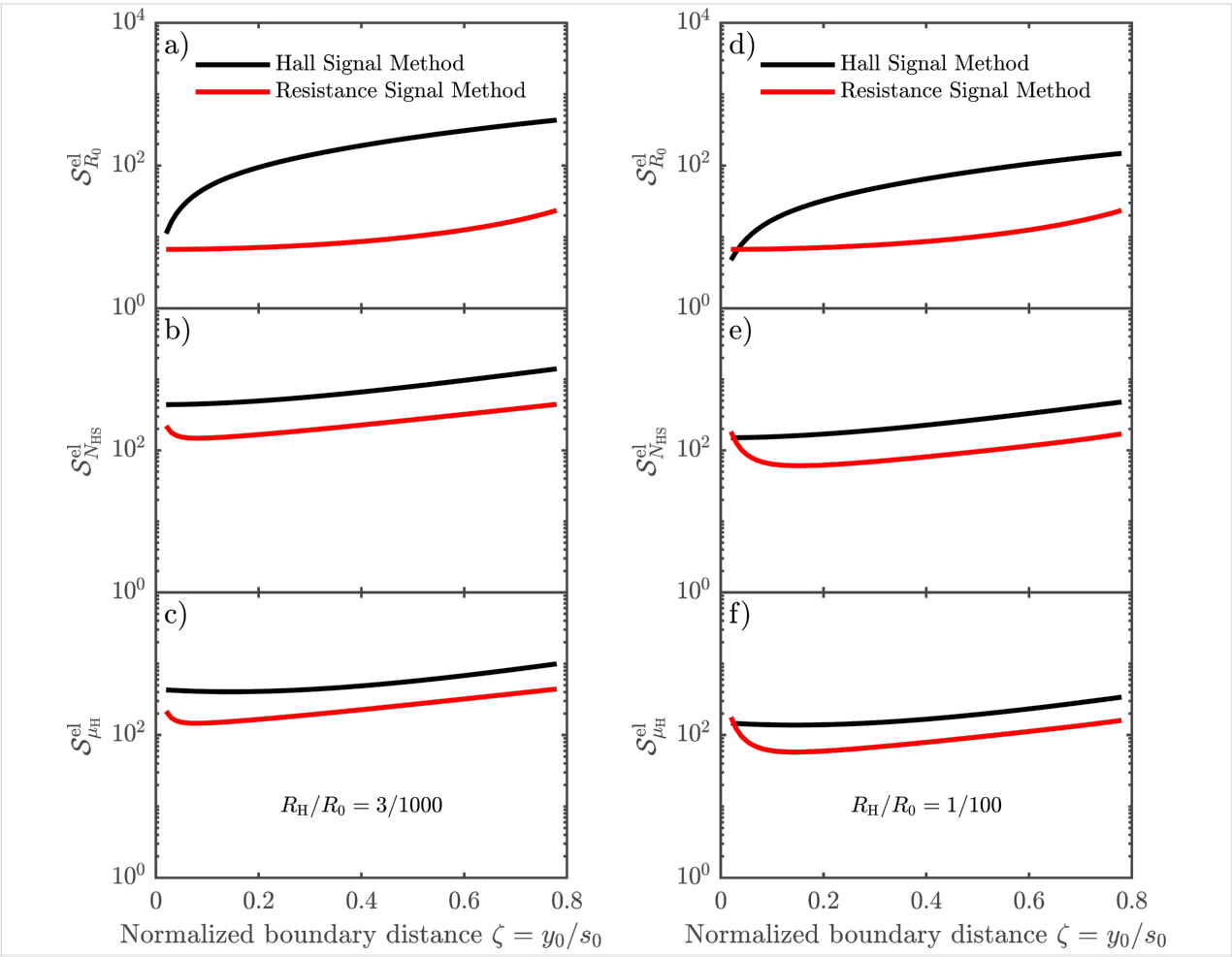



**Figure 6:** Effective sensitivity $\mathcal{S}_{\beta}^{\mathrm{el}}$ for the sheet resistance, Hall mobility and Hall sheet carrier density, due to the presence of electrical noise on the measurements, for the Hall signal method and the resistance signal method for (a–c) $R_H/R_0$ = 3/1000 and (d–f) $R_H/R_0$ = 1/100.

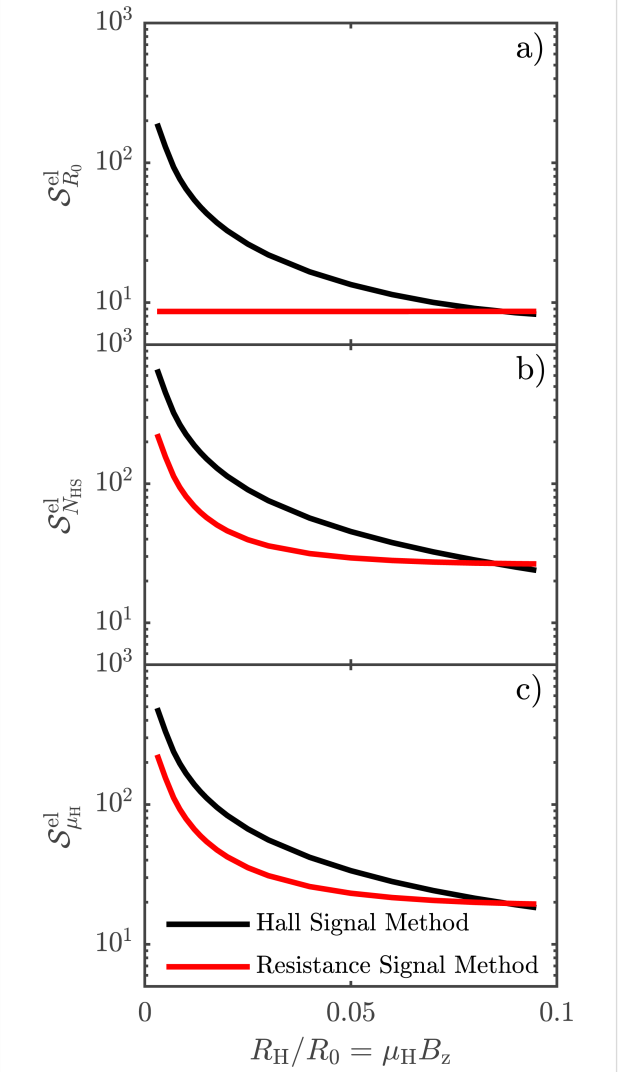



**Figure 7:** Generalization of Figure 6. The sensitivity of each parameter, a) Sheet resistance $R_0$, b) Sheet carrier density $N_{HS}$ and c) Hall mobility $\mu_H$, to electrical noise investigated for varying $R_H/R_0$ ratio, with the probe placed at a distance of $y_0 = 0.4s_0$ away from the insulating boundary.

$R_H/R_0$ ratio. This makes sense, since the magnitude of the Hall signal $\Delta R_{BB'}$ compared to the resistance signal $R_m$ increases with the ratio $R_H/R_0$. Now consider the parameters as extracted from the resistance signal method, indicated by the red lines in Figure 7a–c. $\mu_H$ and $N_{HS}$ display a similar behaviour as their counterparts in the Hall signal method, although with considerably lower magnitude errors, for the same reason as we have outlined previously. The error on $R_0$ for the resistance signal method (Figure 7a) displays a behaviour radically different from the others. The reason is that $R_0$ for the resistance signal method is determined completely without the influence of the Hall signal. Thus, a higher magnitude Hall signal will not result in a reduction of the uncertainty of $R_0$. Instead, we see that the error of $R_0$ is almost constant.

In a real measurement, both position errors and electrical noise are present, and thus the total relative standard deviation of β is

$$\sigma_\beta^{\mathrm{rel,tot}} = \sqrt{\left(\mathcal{S}_\beta^{\mathrm{pos}} \frac{\sigma_{\mathrm{pos}}}{s_0}\right)^2 + \left(\mathcal{S}_\beta^{\mathrm{el}} \frac{\sigma_v}{IR_0}\right)^2}, \qquad (14)$$

where either the first or the second term is dominant depending on the measurement conditions.

## Experimental

Measurements were performed using a microHall-A300 tool from CAPRES A/S and an M7PP with an electrode pitch of 10 µm. The M7PP used consisted of nickel-coated poly-silicon cantilever electrodes extending from the edge of a silicon die. A magnetic field with the flux density $B_z$ = 600 mT was applied perpendicular to a boron-doped ($10^{15}$ cm$^{-2}$) shallow-junction Si sample. The probe was placed nominally 4 µm from the insulating boundary during measurements, i.e., $y_0/s_0 = 0.2$. A total of 150 engages was performed parallel to the insulating boundary, keeping the distance between the probe and insulating boundary constant. At each point, 75 configurations using A, A', B and B' configurations were measured; 25 for each of the sub-probes 1357, 1234 and 4567. The different parameters were then extracted using both the resistance signal method and the Hall signal method. The mean extracted values, as well as the standard deviations for each parameter are shown in Table 1.

**Table 1:** Mean values and standard deviations for the sheet resistance, Hall sheet carrier density and Hall mobility. The measurements were performed under 600 mT flux density and extracted using the resistance signal method and the Hall signal method.

| Method | $R_0 \pm \Delta R_0$ Ω | $N_{HS} \pm \Delta N_{HS}$ $10^{14}$ cm$^{-2}$ | $\mu_H \pm \Delta\mu_H$ cm$^2$/(Vs) |
|---|---|---|---|
| Hall signal | 284 ± 10 | 3.99 ± 0.34 | 56.8 ± 3.0 |
| resistance signal | 284 ± 2 | 3.95 ± 0.19 | 56.0 ± 2.4 |

Table 1 shows that the standard deviations for the resistance signal method are all lower than the corresponding standard deviations found for the Hall signal method. Based on the discussion about the sensitivities to both position errors and electrical noise, this meets the expectations. When a nominal distance to the edge of 4 µm is used during measurements, the resistance signal method should be the most accurate in all cases, according to Figure 5. Furthermore, it is observed that the largest relative deviations are found on the sheet carrier densities and the smallest on the sheet resistances, for both methods. This is also in line with our expectations. Finally, we find that the measurement results correspond to the case where the error is dominated by electrical noise.

## Conclusion

In this paper, we have presented a variable probe pitch method well-suited for characterization purposes in the development of nanoelectronic materials. We have compared two different analysis methods to obtain the electrical parameters $R_0$, $\mu_H$ and $N_{HS}$ from MHE measurement data. We have shown that the resistance signal method is more precise when measuring close to the insulating boundary of a sample, whereas the precision of the Hall signal method is better farther away from such a boundary, when static position errors are present. Furthermore, we have calculated the sensitivity of each method to electrical noise, and the resistance signal method proved superior. Finally, we presented MHE measurements on a B-doped Si ultra shallow junction and the experimental results confirmed the theoretical conclusions, since the standard deviations on the parameters were smaller for the resistance signal method, compared to those found for the Hall signal method.

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# Phosphorus monolayer doping (MLD) of silicon on insulator (SOI) substrates

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## Abstract

This paper details the application of phosphorus monolayer doping of silicon on insulator substrates. There have been no previous publications dedicated to the topic of MLD on SOI, which allows for the impact of reduced substrate dimensions to be probed. The doping was done through functionalization of the substrates with chemically bound allyldiphenylphosphine dopant molecules. Following functionalization, the samples were capped and annealed to enable the diffusion of dopant atoms into the substrate and their activation. Electrical and material characterisation was carried out to determine the impact of MLD on surface quality and activation results produced by the process. MLD has proven to be highly applicable to SOI substrates producing doping levels in excess of $1 \times 10^{19}$ $cm^{-3}$ with minimal impact on surface quality. Hall effect data proved that reducing SOI dimensions from 66 to 13 nm lead to an increase in carrier concentration values due to the reduced volume available to the dopant for diffusion. Dopant trapping was found at both Si–$SiO_2$ interfaces and will be problematic when attempting to reach doping levels achieved by rival techniques.

## Introduction

Aggressive device scaling in the sub-20 nm region has resulted in a number of techniques that were previously essential being deemed detrimental to current and future device production. Semiconductor substrates require doping to reduce their resistivity and enable their use in electronic devices such as metal-oxide semiconductor field-effect transistors (MOSFETs). Traditionally, ex situ doping was carried out using ion implantation, which suffers from several downsides when used on sub-10 nm devices and with three-dimensional architectures [1,2]. The main issues with ion implantation are that it introduces crystal

damage that cannot be annealed out of these extremely small sub-10 nm devices, and that it is unable to conformally dope three-dimensional nanostructures due to the directionality of the technique. Ion implantation operators have devised several methods to counter these issues such as hot implantations but have shown only moderate success [3,4].

The introduction of crystal damage has major consequences when preparing devices for applications in the electronics industry such as CMOS. The short-channel effect (SCE) becomes more profound with reduced device dimensions and when combined with crystal damage leads to high leakage currents, which result in elevated power consumption. Therefore, it is essential for future device scaling that a means of damage-free, conformal doping is established, and this is where monolayer doping (MLD) appears to have potential to succeed.

MLD was pioneered by Javey and co-workers [5] in 2008 and has subsequently been used to dope multiple substrate types such as silicon [5-8], germanium [9-11] and others [12]. MLD involves the use of surface chemistry to provide a source of dopant atoms for diffusion into the substrate. Figure 1 shows a schematic version of the steps involved in a MLD process. The most commonly used reaction involves the hydrosilylation of an allyl-containing dopant molecule by a hydrogen-terminated silicon surface (produced using hydrofluoric acid). A capping layer is then applied to the sample followed by thermal treatment to promote diffusion of the dopant atoms into the silicon substrate while also providing enough energy to activate them in the crystal structure. By contrast, Ye et al. have recently proposed a monolayer contact doping (MLCD) process without the need for a capping layer [13].

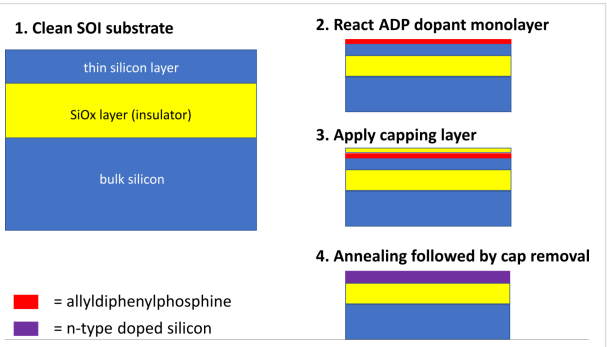



**Figure 1:** Schematic depicting MLD processing applied to silicon on insulator wafers. It shows monolayer formation (allyldiphenylphosphine dopant molecules) followed by capping and finally thermal annealing and cap removal to provide an n-type doped silicon layer.

This paper will examine the application of phosphorus MLD to silicon on insulator (SOI) substrates with nanoscale dimensions (sub-66 nm silicon layer). Bulk silicon transistors encounter difficulties when scaled below 20 nm due to SCE and significant leakage currents, which increase their power consumption. SOI and three-dimensional finFET structures are two means of device scaling that are currently being pursued by the electronics community. Planar, fully depleted SOI (FD-SOI) has been used to provide a more cost-effective scaling mechanism than FinFET alternatives. Although initial wafer cost is higher for SOI compared to bulk silicon, which is used in finFETs, the further masking and etching required for fin production is both complex and expensive. SOI allows for excellent electrostatic control of the channel without needing to dope this channel. Ultra-thin body SOI is also known to be high speed with low power consumption and low parasitic capacitance [14]. SOI doping has applications in a variety of fields including electronics, thermoelectrics and photovoltaics. MLD is capable of damage-free source/drain doping of planar SOI. There have been no previous publications of MLD on SOI substrates, which due to their confined dimensions, may provide an opportunity to limit dopant atom diffusion and therefore achieve active carrier concentrations greater than those that would be expected in bulk silicon.

## Results and Discussion

1 × 1 cm bulk p-type silicon and SOI samples were cut, and hydrogen-terminated using 2% hydrofluoric acid. The functionalization procedure was then carried out as outlined in the Experimental section. Allyldiphenylphosphine (ADP) was used as the dopant molecule in view of its commercially availability and relatively small size. ADP also minimizes the possibility of multilayer formation because it contains two unreactive phenyl functional groups.

Initial tests were carried out to determine whether a capping layer was necessary when carrying out phosphorus MLD. This was done using bulk silicon samples. Electrochemical capacitance–voltage (ECV) profiling is a technique that analyses the quantity of active dopant atoms present in a substrate as a function of the depth. Figure 2 shows that the application of a capping layer is necessary to achieve maximum dopant incorporation when carrying out P-MLD using ADP as the dopant molecule. $SiO_2$ was chosen as capping material due to the poor diffusivity of P through $SiO_2$, which would favour the preferential diffusion of P into the silicon substrate. Without the protection of a capping layer the dopant monolayer is essentially "burnt" off during high-temperature annealing. Cap removal was carried out using a standard buffered oxide etch.

Atomic force microscopy (AFM) was used to acquire high-resolution topographic images to evaluate the surface quality throughout MLD processing. Starting wafers were of good quality showing roughness values (RMS) below 0.2 nm

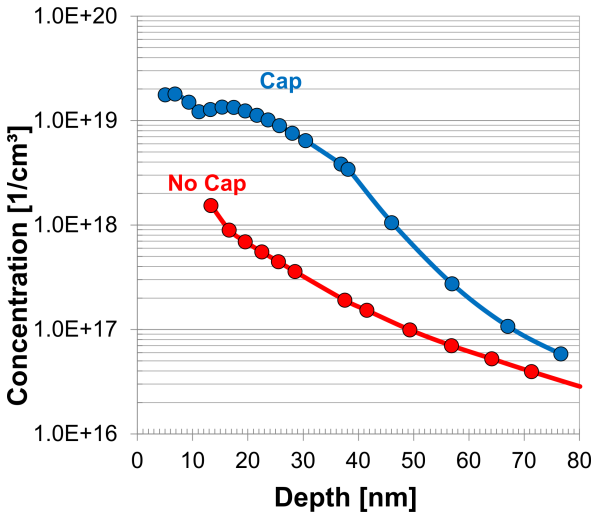



**Figure 2:** Electrochemical capacitance–voltage profile showing the impact of applying a $SiO_2$ capping layer for the duration of the annealing process. Both samples were annealed at 1050 °C for 5 s (the inset shows the allyldiphenylphosphine dopant molecule).

(Figure 3). After MLD processing, the roughness values slightly increase to approximately 0.3 nm but this may be due to small oxide fragments on the surface, which remain from the cap removal process. Otherwise the surface quality remains relatively smooth. These values are important for both further analysis and industrial applications of MLD on SOI. The carrier-concentration analysis techniques ECV and Hall effect measurement both require high-quality surfaces and substrates to provide accurate data. Furthermore, from an industrial point of view it is important that surface quality remains good to ensure reproducibility over large sample quantities.

P-MLD processing was carried out on 66 nm SOI wafers through the methods outlined in the Experimental section. The active carrier concentration levels shown in Figure 4 approach $2 \times 10^{19}$ $cm^{-3}$, which correlate with the results seen during the initial capping test carried out on bulk substrates. This data shows that, as expected, MLD is applicable to SOI substrates. A comparison with 13 nm substrates will demonstrate the effect of confining the dopant diffusion.

It is also important to note that functionalization was carried out using a low concentration of ADP (0.1 M = 2% v/v). Even at these low levels it was found on bulk silicon substrates that ADP produced optimal active carrier concentration levels after processing with a functionalization of 3 h shown in Figure 5.

13 nm SOI samples were prepared and MLD-doped through the methods outlined in the Experimental section. ECV was not

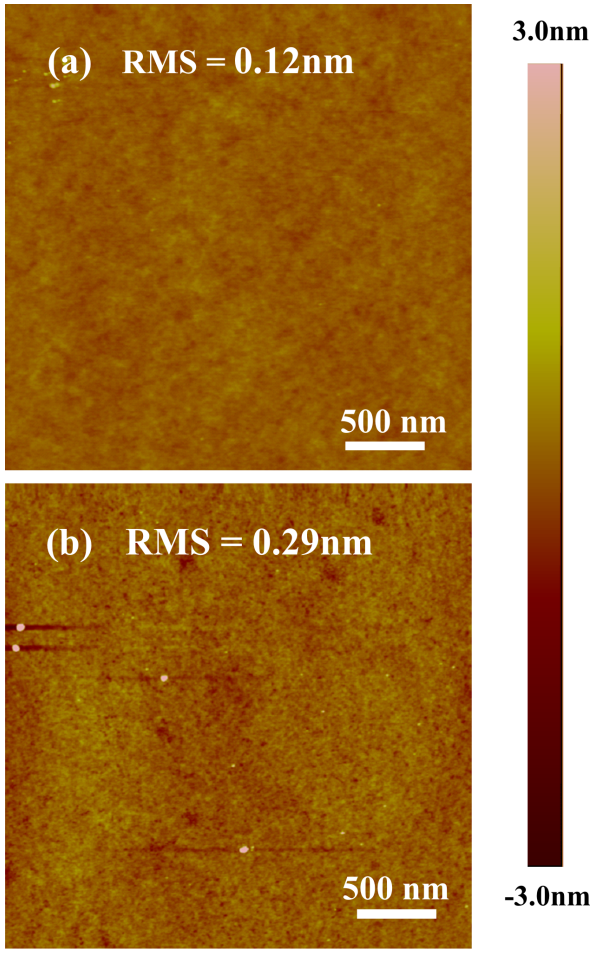



**Figure 3:** AFM images of (a) as received SOI (b) SOI after MLD processing.

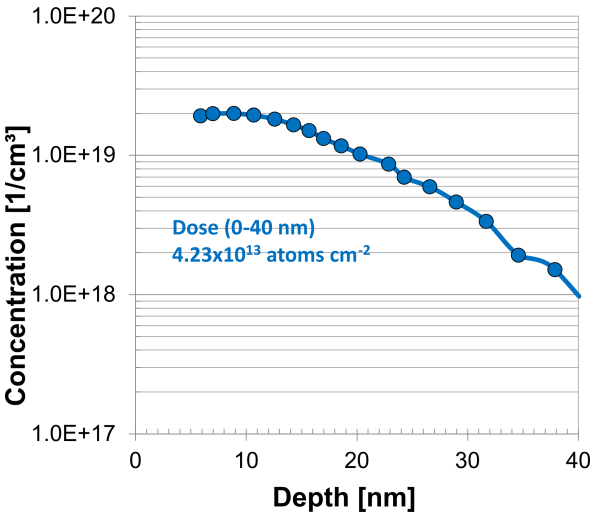



**Figure 4:** ECV plot of active carrier concentrations in a 66 nm SOI after MLD using a 50 nm sputtered $SiO_2$ cap and annealing at 1050 °C for 5 s.

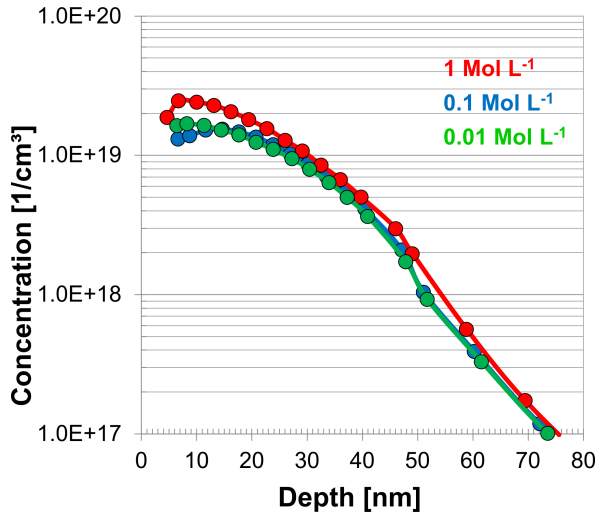



**Figure 5:** ECV plot of active carrier concentrations using bulk silicon samples to analyse the variation of the molecule concentration during functionalization. A 50 nm sputtered $SiO_2$ cap and annealing at 1050 °C for 5 s was used for all samples.

applicable to analyse active carrier concentrations present in these samples due to their inability to etch. When etching n-type doped semiconductors, ECV requires the application of a voltage to draw holes to the surface and enable the dissolution of the semiconductor into the electrolyte. Applying this voltage near the insulator layer becomes problematic and prevents etching and analysis in this region. Hall effect measurements were instead used, which required careful handling during wet-chemistry functionalization due to the precise dimensions needed for analysis. The Hall measurement system applies current and magnetic field and measures voltages and resistances. It then infers mobility and carrier properties from these measurements. The sheet resistivity ($\rho_s$) is directly measured first by the four-point method, followed by the sheet Hall coefficient (sheet Hall resistance divided by magnetic field) as measured by Hall effect, $R_{HS} = V_H/(I{\cdot}B)$, where $V_H$ is the measured Hall voltage, $I$ is the applied current and $B$ is the applied magnetic field. Since $\rho_s$ and $R_{HS}$ are now directly measured and $R_{HS} = \rho_s{\cdot}\mu_H$, we can now infer the Hall mobility, $\mu_H$. The sheet carrier concentration ($n_s$) is obtained from $R_{HS} = h_f/n_s{\cdot}e$, where $e$ is the electron charge. In dc mode, the carrier type is determined by the sign of the Hall voltage (negative = n-type, positive = p-type). In ac mode, the carrier type is determined by the phase of the Hall voltage (±180° = n-type; ±0° = p-type). Finally, applying a known or assumed thickness can convert these sheet properties to thickness-dependent properties.

A summary of the key data found with Hall effect analysis is shown in Table 1 with a more comprehensive data set available in Table S1 (Supporting Information File 1). The sheet carrier concentration (CC, dose) values, from ac mode, are virtually the same for both the 13 and 66 nm substrates. This is due to the overall dose available being limited by surface coverage of the ADP dopant molecule. Consistent dose values produced by MLD are desirable when compared with fluctuations seen using other techniques. However, the volume of the 13 nm samples is significantly less than that of the 66 nm sample, which leads to a higher carrier concentration (CC, $n$; concentration = dose/thickness). This is a very positive outcome. As a result of the increased carrier concentration the mobility drops, which is expected for silicon [15].

**Table 1:** Hall effect data of 66 nm and 13 nm MLD-doped SOI.

| property | unit | 66 nm sample | 13 nm sample |
|---|---|---|---|
| mobility $\mu_H$ | $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ | 125.72 | 61.79 |
| sheet CC | $cm^{-2}$ | $2.3 \times 10^{13}$ | $2.26 \times 10^{13}$ |
| CC, $n$ | $cm^{-3}$ | $3.49 \times 10^{18}$ | $1.74 \times 10^{19}$ |

## Dopant trapping

MLD is a surface-diffusion technique in which the dopant source is applied to the substrate surface and requires further thermal treatment to promote diffusion into the substrate and to electrically activate these dopant atoms. Although this process sounds trivial, there are numerous issues that can arise and prevent the movement of the dopant into the target area. In the case of silicon doping the most prominent issue is the silicon oxide formation at the surface. Phosphorus diffuses through silicon oxide significantly slower than through silicon [16,17]. Although it has been shown that hydrogen-terminated silicon re-oxidizes relatively slowly when stored at room temperature in air [3], the elevated temperatures required for MLD processing carried out in the liquid phase enhances this re-oxidation. Therefore, precautions are taken to ensure a minimal re-oxidation, i.e., solvents are thoroughly degassed, and processing is carried out in a $N_2$ environment using a Schlenk line.

XPS analysis of samples immediately after functionalization indicated that surface oxidation had taken place during this process despite the care taken to avoid oxidation. The Si 2p peak shown in Figure 6 has a sub-peak at approximately 104 eV, which is a result of the presence of $SiO_2$. The presence of even this small amount of $SiO_2$ has the ability to inhibit P diffusion into the Si substrate.

MLD-doped 66 nm SOI was further examined using secondary ion mass spectrometry (SIMS) to attain a more detailed view of total dopant distribution in the substrate, which is complementa-

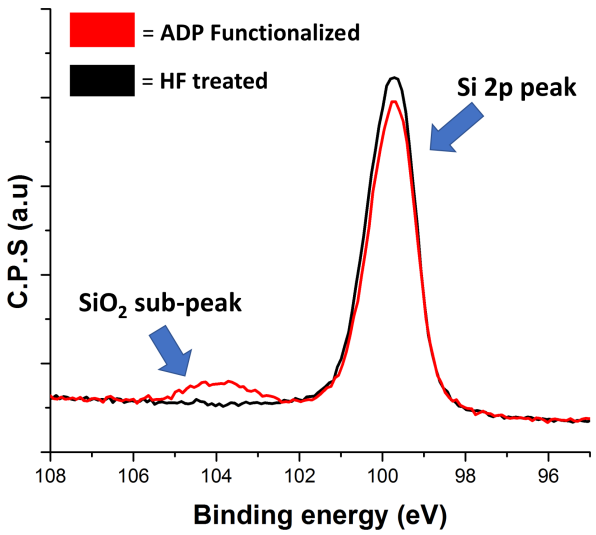



**Figure 6:** X-ray photoelectron spectroscopy (XPS) study showing that there is a degree of surface oxidation after functionalization procedure even when carried out under inert conditions.

ry to previous measurements of active carrier concentrations through ECV. Data shown in Figure 7 correlates well with Hall effect and ECV measurements shown previously, with P concentration levels of $2 \times 10^{19}$ $cm^{-3}$ from 2 nm onwards, this shows that the majority of dopant atoms from this point are electrically active. The maximum levels found from SIMS were in the first 2 nm with values approaching $3 \times 10^{20}$ $cm^{-3}$. However, due to the inaccuracy of SIMS in this region it is difficult to assess these values. One possible reason for these elevated values may be dopant trapping by $SiO_2$ during the annealing process. The surface oxidation found after functionalization (Figure 6) has the potential to inhibit diffusion into the substrate. Other research groups [7,8,18], working on P diffusion doping using a variety of techniques have also seen limitations at $2 \times 10^{19}$ $cm^{-3}$.

This was further examined by using longer annealing times of 10 and 100 s. Figure S1 (Supporting Information File 1) shows that this leads to an increased dose with maximum active carrier concentration levels remaining at $2 \times 10^{19}$ $cm^{-3}$. This leads us to believe that the presence of $SiO_2$ near the sample surface may be inhibiting the in-diffusion of the P dopant atoms.

The final noteworthy aspect of this SIMS profile is the peak seen at the silicon–insulator interface. A spike in P concentration is seen showing that it may also be trapped at this point in the substrate. This spike could be explained by the slower diffusion of P in $SiO_2$ compared to Si and a similar feature has been seen previously after ion implantation of SOI substrates [19]. A previous work by Mastromatteo et al. [20] examining P implantation of silicon nanocrystals embedded into $SiO_2$ attributed a similar P peak to interface effects. It is unclear as to whether the silicon to insulator interface in these SOI substrates will behave in a manner similar to that of the silicon nanocrystals. In order to attain a more detailed understanding of this interface peak a more comprehensive study of this back interface would have to be undertaken.

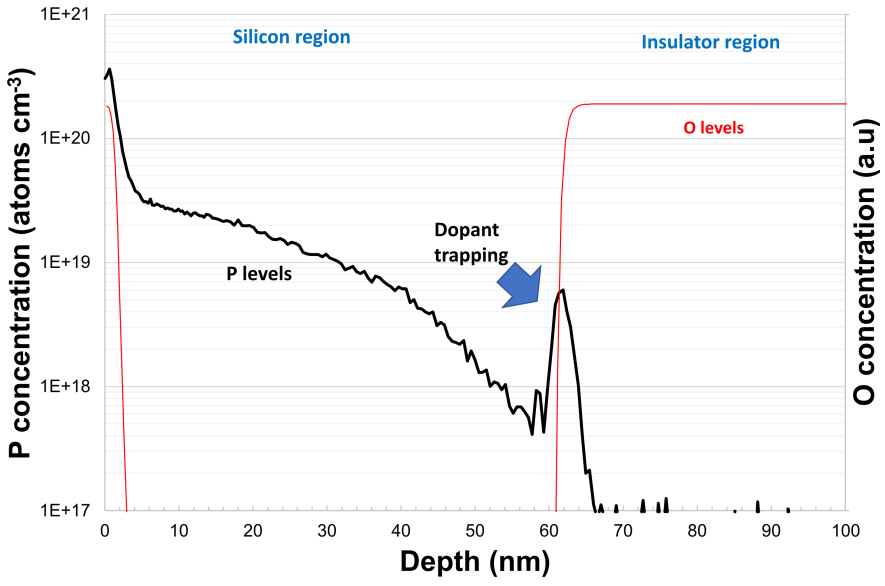



**Figure 7:** Secondary ion mass spectrometry analysis of a P-MLD-doped 66 nm silicon on insulator substrate. Blue line: P concentration, red line: O concentration.

## Conclusion

This study has demonstrated the first application of MLD to SOI substrates. Active carrier concentration levels attained in these substrates were consistently in the region of $2 \times 10^{19}$ $cm^{-3}$. Reducing the SOI dimensions did lead to an increase in carrier concentration (CC, *n*) found using Hall effect measurements. Further reducing the SOI dimensions into the sub-10 nm region will provide interesting knowledge around the application of P-MLD to ultra-thin SOI. Surface analysis showed that MLD processing caused minimal impact on sample surface quality and previous studies have also demonstrated the gentle nature of MLD on crystal quality. Dopant trapping at the Si–$SiO_2$ interface appears to be a significant issue when applying MLD to SOI substrates. Considerable quantities of dopant atoms appear to be remaining in the surface region due to the presence of $SiO_2$, which slows P diffusion. The use of more advanced techniques such as laser, flash lamp, and microwave annealing may solve this issue and allow for higher carrier concentration levels approaching the solid-solubility limits to be achieved in silicon.

## Experimental

### Substrate preparation

SOI samples were degreased through sonication in acetone for 120 seconds followed by a dip in 2-propanol and drying under a stream of nitrogen. Samples were then placed in a 2% HF solution for a period of 10 seconds to provide a hydrogen terminated surface. Following this HF treatment, the Si samples were dried under a stream of nitrogen and promptly placed under inert conditions in the Schlenk apparatus to prevent re-oxidation.

### Functionalization with ADP

All reaction steps were carried out under inert conditions on a Schlenk line apparatus. A solution of ADP in mesitylene (100 µL in 5 mL) was degassed using multiple freeze–pump–thaw cycles followed by transfer to the reaction flask containing the hydrogen-terminated silicon sample. This reaction flask was connected to a condenser that enabled reflux conditions during the 3 h heating period.

### Capping and annealing

A 50 nm $SiO_2$ capping layer was sputtered on all samples prior to thermal treatments. Rapid thermal annealing was carried out allowing for temperatures greater than 1000 °C for time periods of less than 10 s, capable of producing ultra-shallow doping profiles. Capping layers were removed using a standard buffered-oxide etch (BOE). Optimal annealing conditions to provide high dose and active carrier concentrations while limiting the diffusion and junction depth were examined in Figure S1 and Figure S2 (Supporting Information File 1), which lead to the use of a 1050 °C annealing for a time period of 5 s for all applications to SOI.

### Characterisation

Atomic force microscopy was carried out in tapping mode at room temperature to analyse the surface quality throughout the MLD process. ECV profiling (CVP21 Profiler) was used to determine the active carrier concentrations in the samples after the doping process was completed. Ammonium hydrogen difluoride (0.1 M) was chosen as a suitable electrolyte/etchant as it can remove the native oxide layer without etching into the underlying substrate under neutral conditions. Controlled-voltage etching was carried out with step widths of 2–5 nm. Secondary ion mass spectrometry data was acquired on a Phi Adept 1010 using a 0.5–1.0 keV $Cs^+$ bombardment with negative ion detection.

### X-ray photoelectron spectroscopy

XPS spectra were acquired on an Oxford Applied Research Escabase XPS system equipped with a CLASS VM 100 mm mean radius hemispherical electron energy analyser with a triple-channel detector arrangement in an analysis chamber with a base pressure of $5.0 \times 10^{-10}$ mbar. Survey scans were acquired between 0 and 1400 eV with a step size of 0.7 eV, a dwell time of 0.3 s and a pass energy of 50 eV. Core-level scans were acquired at the applicable binding energy range with a step size of 0.1 eV, dwell time of 0.1 s and pass energy of 20 eV averaged over 10 scans. A non-monochromated Al Kα X-ray source at 200 W power was used for all scans. All spectra were acquired at a take-off angle of 90° with respect to the analyser axis and were charge-corrected with respect to the C 1s photoelectric line by rigidly shifting the binding energy scale to 284.8 eV. Data were processed using CasaXPS software where a Shirley background correction was employed.

### Hall effect measurements

Room temperature Hall effect measurements are performed using a controllable electromagnet in a LakeShore Model 8404 Hall effect measurement system (HMS) with dc and ac magnetic field capability in the range of ±1.7 T for dc, and of 1.2 T RMS (ac, 50/100 mHz), respectively. The ac magnetic field mode works in combination with a high-resolution lock-in amplifier that filters out all dc error components and uses phase analysis to remove ac error components. As a consequence, the ac results are generally more accurate that the dc results. Fitted with a high-resistance unit, the HMS can deal with many material systems that have low mobility, high resistivity and low carrier concentrations. As well as Hall effect measurements, the HMS also performs checks for ohmic behaviour and four-point resistivity measurements, and combines all-current/field-reversal techniques, optimisation methods and averaging

between all geometries to remove most major error components and obtain an accurate Hall voltage assessed against the signal-to-noise (SNR) accuracy obtained [21]. For all samples assessed in this work, the coupon size is ca. 1 cm × 1 cm with four pressure probe metal contacts placed in the corners of the coupon, thus creating a van der Pauw structure [22]. The Hall factor ($h_f$) is set to unity and the ac frequency is 100 mHz. We assume a uniform thickness with a uniform response across the material thickness. Moreover, the material is assumed to not have a dominant interlayer to be isolated electrically. If thickness-dependent properties are reported, we assume the thickness reported is correct.

## Supporting Information

Comprehensive Hall effect analysis data and ECV of annealing variation experiments on bulk silicon.

### Supporting Information File 1

Additional experimental data.
[https://www.beilstein-journals.org/bjnano/content/supplementary/2190-4286-9-199-S1.pdf]

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BEILSTEIN JOURNAL OF NANOTECHNOLOGY

# Intrinsic ultrasmall nanoscale silicon turns n-/p-type with $SiO_2/Si_3N_4$-coating

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## Abstract

Impurity doping of ultrasmall nanoscale (usn) silicon (Si) currently used in ultralarge scale integration (ULSI) faces serious miniaturization challenges below the 14 nm technology node such as dopant out-diffusion and inactivation by clustering in Si-based field-effect transistors (FETs). Moreover, self-purification and massively increased ionization energy cause doping to fail for Si nano-crystals (NCs) showing quantum confinement. To introduce electron- (n-) or hole- (p-) type conductivity, usn-Si may not require doping, but an energy shift of electronic states with respect to the vacuum energy between different regions of usn-Si. We show in theory and experiment that usn-Si can experience a considerable energy offset of electronic states by embedding it in silicon dioxide ($SiO_2$) or silicon nitride ($Si_3N_4$), whereby a few monolayers (MLs) of $SiO_2$ or $Si_3N_4$ are enough to achieve these offsets. Our findings present an alternative to conventional impurity doping for ULSI, provide new opportunities for ultralow power electronics and open a whole new vista on the introduction of p- and n-type conductivity into usn-Si.

## Introduction

Impurity doping of silicon (Si) has been a key technique and prerequisite for Si-based electronics for decades [1]. Miniaturization in Si ultralarge scale integration (ULSI) became increasingly difficult as device features approached the characteristic lengths of dopant out-diffusion, clustering and inactivation [2]. The considerable broadening of dopant profiles from drain/source regions into gate areas persists [3]. Moreover, required ULSI transistor functionality and emerging applications of Si-nanocrystals (NCs) [4] unveiled additional doping issues: self-purification [5,6], suppressed dopant ionization [7,8] and dopant-associated defect states [8,9].

Modulation doping – i.e., doping of materials adjacent to semiconductors which then provide free carriers to the unperturbed semiconductor – was first used for group III–V semiconductor combinations such as GaAs/AlAs in the late 1970s [10]. Recently, Si modulation doping of adjacent dielectric layers based on nitrides [11] and oxides [12], in analogy to modulation doping of III–V semiconductors, were shown to be an alternative to conventional impurity doping.

It would be ideal to achieve electron- (n-) or hole- (p-) type conductivity in usn-Si without doping, thereby avoiding all dopant-related issues mentioned above. Such conductivity can be induced by an energy offset ($\Delta E$) of the same electronic states (lowest unoccupied molecular orbital (LUMO) or highest occupied molecular orbital (HOMO)) between different regions of the same usn-Si system [13,14]. This concept eliminates doping altogether, leading to a lower inelastic carrier scattering rate and higher carrier mobility which allow for decreased heat loss and bias voltages in ULSI. Such properties enable Si-FET technology to work at even smaller structure sizes, potentially enabling Moore's law to reach the Si-crystallization limit of ca. 1.5 nm [15].

In our present work, we prove by hybrid-density functional theory (h-DFT) simulations and synchrotron-based long-term ultraviolet photoelectron spectroscopy (UPS) that usn-Si indeed can have a massive $\Delta E$ of their electronic density of states (DOS) when embedded in $SiO_2$ or $Si_3N_4$. We use further h-DFT results of a Si-nanowire (NWire) covered in $SiO_2$ and $Si_3N_4$ to examine the device behaviour of an undoped Si-NWire FET based solely on CMOS-compatible materials (e.g., Si, $SiO_2$, $Si_3N_4$) using the nonequilibrium Green's function (NEGF) approach.

Following an explanation of the theoretical and experimental methods used, we turn to results for Si-NCs obtained from h-DFT. Here, we focus on the electronic structure of Si-NCs as a function of the embedding dielectric and its thickness of up to 3 monolayers (MLs). The latter dependence requires the use of NCs to keep the h-DFT computation effort practicable; NWires with more than 1 ML dielectric embedding are beyond the feasible computation effort at the level of accuracy we use. As an ultimate theoretical test, we present h-DFT results of two Si-NCs, one embedded in $SiO_2$ and the other embedded in $Si_3N_4$, presenting the entire system under investigation within one approximant. An interface charge transfer (ICT) of electrons from the usn-Si volume to the anions of the embedding dielectric – nitrogen (N) or oxygen (O) – is at the core of the energy shift [14]. We explain the shift of usn-Si electronic states towards the vacuum level $E_{vac}$ when embedded in $Si_3N_4$ and further below $E_{vac}$ when embedded in $SiO_2$ by the quantum chemistry of N and O with respect to Si. The next section contains experimental results, namely the thickness determination of embedded Si nanowells (NWells) by transmission electron microscopy (TEM) and the measurement of the highest occupied DOS over energy for Si-NWell samples embedded in $SiO_2$ or $Si_3N_4$ by synchrotron-based long-term UPS. With this experimental confirmation of our h-DFT results, we present the concept of undoped Si-NWire field-effect transistors (FETs). We show further h-DFT results of a Si-NWire of 5.2 nm length and 1.4 nm diameter, terminated to 50% with 1 ML of $Si_3N_4$ ($NH_2$ groups) and to 50% with 1 ML of $SiO_2$ (OH groups). These h-DFT results deliver key input data to NEGF device simulations as a proof-of-concept for the undoped Si-NWire FET. A wealth of information on h-DFT accuracy as compared to experiment, details of UPS measurements and NEGF are contained in Supporting Information File 1.

## Experimental

### h-DFT material calculations

Hybrid-DFT calculations were carried out in real space with a molecular orbital basis set (MO-BS) and both Hartree–Fock (HF) and h-DFT methods as described below, employing the Gaussian03 and Gaussian09 program packages [16,17]. Initially, the MO-BS wavefunction ensemble was tested and optimized for stability with respect to describing the energy minimum of the approximant (variational principle; stable = opt) with the HF method using a Gaussian-type 3-21G MO-BS [18] (HF/3-21G). This MO wavefunction ensemble was then used for the structural optimisation of the approximant to arrive at its most stable configuration (maximum integral over all bond energies), again following the HF/3-21G route. Using these optimized geometries, their electronic structure was calculated again by testing and optimizing the MO-BS wavefunction ensemble with the B3LYP hybrid DF [19,20] and the Gaussian-type 6-31G(d) MO-BS which contains d-polarization functions (B3LYP/6-31G(d)) [21] to describe the strong polar nature

of atomic bonds of Si to O and N. The root mean square (RMS) and peak force convergence limits for all atoms were $3 \times 10^{-4}$ Ha/$a_0$ (Hartrees per Bohr radius) or 80 meV/nm and $4.5 \times 10^{-4}$ Ha/$a_0$ or 120 meV/nm, respectively. Tight convergence criteria were applied to the self-consistent field routine. Ultrafine integration grids were used throughout. During all calculations, no symmetry constraints were applied to MOs. An extensive accuracy evaluation can be found in the Supporting Information File 1 of this article and elsewhere [13,14,22]. The approximants and MOs were visualized with GaussView 5 [23]. The electronic DOS were calculated from MO eigenenergies, applying a Gaussian broadening of 0.2 eV.

## Sample preparation

Samples comprising a $Si_3N_4$-embedded NWell were fabricated by plasma-enhanced chemical vapour deposition (PECVD) using $SiH_4$+$NH_3$+$N_2$ for $Si_3N_4$ and $SiH_4$+Ar for amorphous Si [24]. As substrates, n-type Si wafers (Sb doping, 5 to $15 \times 10^{-3}$ Ω cm) of (111)-surface orientation underwent wet-chemical cleaning. After deposition the wafers were annealed in a quartz tube furnace for 1 min at 1100 °C in pure $N_2$ ambient to induce Si crystallization. Subsequently, the samples were $H_2$-passivated at 450 °C for 1 h. A 4.5 nm thick $Si_3N_4$ spacer layer served to suppress excited electrons from the Si wafer to interfere with electrons from the Si-NWell during UPS.

Samples comprising a $SiO_2$-embedded NWell were processed by etching the top c-Si layer of an Si-on-insulator (SOI) wafer with 200 nm buried $SiO_2$ (BOX) down to ca. 3 nm. The subsequent oxidation resulted in a 1.7 nm Si-NWell and 1.5 nm $SiO_2$ capping.

Si reference samples were processed by etching a 5 to $15 \times 10^{-3}$ Ω cm Sb-doped n-type (111)-Si wafer in buffered hydrofluoric acid, and the sample was immediately mounted under a $N_2$-shower then swiftly loaded into the ultrahigh vacuum (UHV) annealing chamber.

All NWell samples were contacted via a lateral metal contact frame on the front surface which was processed by photolithographical structuring, wet-chemical mesa etching and thermal evaporation of Al. The reference Si-wafer was contacted directly on its front surface.

## Characterization

UPS measurements were carried out at the BaDElPh beamline [25] at the Elettra Synchrotron in Trieste, Italy, in top-up mode (310 mA electron ring current). All samples were subject to a UHV anneal for 90 min at 500 K to desorb water and air-related species from the sample surface prior to the measurements. Single scans of spectra were recorded over 12 h per NWell sample and subsequently added up for eliminating white noise. Scans for the Si-reference sample were recorded over 2 h and subsequently added up. All NWell samples were exited with a photon energy of 8.9 eV and a photon flux of $2 \times 10^{12}$ $s^{-1}$. The incident angle of the UV beam onto the sample was 50° with respect to the sample surface normal, and excited electrons were collected with an electron analyzer along the normal vector of the sample surface. The energy calibration of the UPS was realized using a tantalum (Ta) stripe in electrical contact to the sample as a work function reference. Further UPS-data of $SiO_2$ and $Si_3N_4$ reference samples as well as UPS signal normalization are available in Supporting Information File 1.

All samples for TEM investigation were capped with a protective $SiO_2$-layer to facilitate the preparation of cross sections by the focused ion beam technique using a FEI Strata FIB 205 workstation. Some samples were further thinned by means of a Fischione NanoMill. The TEM analysis of the cross sections was performed on a FEI Tecnai F20 TEM operated at 200 kV at the Central Facility for Electron Microscopy, RWTH Aachen University, and on the spherical aberration corrected FEI Titan 80-300 TEM operated at 300 kV at Ernst Ruska-Centre, Forschungszentrum Jülich [26].

In addition, the Si-NWell thickness was measured by ellipsometry. The thickness of the Si-NWells in $Si_3N_4$ (in $SiO_2$) were measured using a Woollam M-2000 ellipsometer (ACCURION nanofilm ep4se ellipsometer). All thickness measurements confirmed the values obtained from TEM.

## NEGF device simulations

A homemade NEGF simulation program was used for simulating nanoscale device characteristics based on h-DFT results of Si-NWires. The simulations are based on a self-consistent solution of the Poisson and Schrödinger equations on a finite difference grid. A one-dimensional, modified Poisson equation is considered here that provides an adequate description of the electrostatics of wrap-gate nanowire transistors [27]. Buettiker probes, i.e., virtual contacts, are attached to each finite difference site in order to mimic inelastic scattering [28]. To this end, an additional self-consistent calculation of the quasi-Fermi level throughout the device is computed, ensuring that the net current flow into/out of each Buettiker probe is zero. The electrostatics within the gate underlap region has been taken into consideration with a conformal mapping technique that maps the underlap region to a parallel-plate capacitor and allows the extraction of a space-dependent effective oxide thickness that is used in this region. The “doping” due to the presence of the $SiO_2$ coating is taken into consideration as a volume, active dopant concentration (see Supporting Information File 1); the presence of the $Si_3N_4$ layer underneath the gate is accounted for

by an appropriate shift of the threshold voltage of the transistor (see Supporting Information File 1).

## Results and Discussion

### h-DFT calculations of embedded Si nanocrystals, fundamentals of energy offset

For evaluating the energy shift $\Delta E$ of the electronic DOS between usn-Si covered with $SiO_2$ or $Si_3N_4$, we calculated two Si-NCs ($Si_{10}$, 0.8 nm size) within one approximant; one NC is embedded in $SiO_2$ and one NC resides in $Si_3N_4$ (Figure 1). We found earlier that – regarding DFT – $Si_{10}$-NCs are the smallest NCs above the atomic limit below which Si-clusters behave as small molecules in the gas phase [13]. The frontier-OMOs exist within the $Si_3N_4$-embedded Si-NC (Figure 1, inset iii), while the frontier-UMO exists within the $SiO_2$-embedded Si-NC (Figure 1, inset ii), with $\Delta E$ of the occupied frontier MOs of 0.5 eV and of 1 eV for the unoccupied frontier MOs between both NCs. These $\Delta E$ values are smaller when compared to individual embedded NCs (see Figure 2c and Supporting Information File 1) due to the inter-NC distance of merely 1 nm, accounting for some ICT convergence from Si NCs to $SiO_2$ or $Si_3N_4$. From Figure 2c we see that an ICT saturation is evident for ≥2 ML $SiO_2$. This saturation is less apparent when $Si_3N_4$ is applied as the embedding matrix. We explain this behaviour together with the $\Delta E$ by the quantum-chemical properties of Si, N and O.

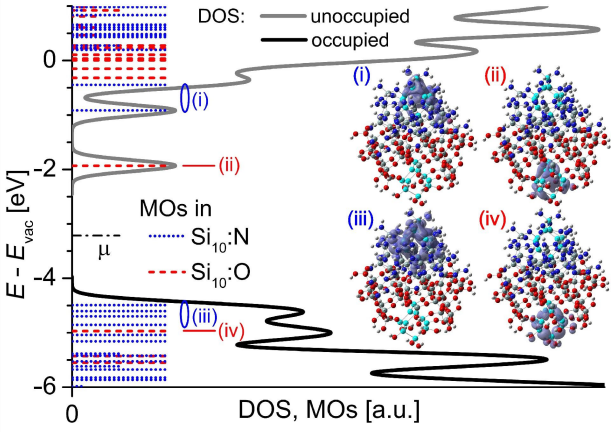



**Figure 1:** Energy offsets with $SiO_2$- and $Si_3N_4$-embedding for one $Si_{10}$-NC (0.8 nm size) embedded in $SiO_2$ and the other $Si_{10}$-NC embedded in $Si_3N_4$ within one approximant. The main graph shows the electronic DOS. MOs localized in $Si_3N_4$- ($SiO_2$-) embedded Si-NC are shown in blue (red); the reduced length of the MOs corresponds to partial localization in $Si_{10}$-NC, with the remainder of the MO being localized within the dielectric. The chemical potential of the entire approximant μ is shown as a dashed-dotted line. Graphs (i) to (iv) show iso-density plots ($1 \times 10^{-3}$ states/$a_0^3$ = 6.76 states/nm$^3$) of frontier MOs marked by (i) to (iv) in the DOS plot. $Si_{10}$-NCs are shown in cyan, Si in $SiO_2$ and $Si_3N_4$ in grey, O in red, N in blue and H in white.

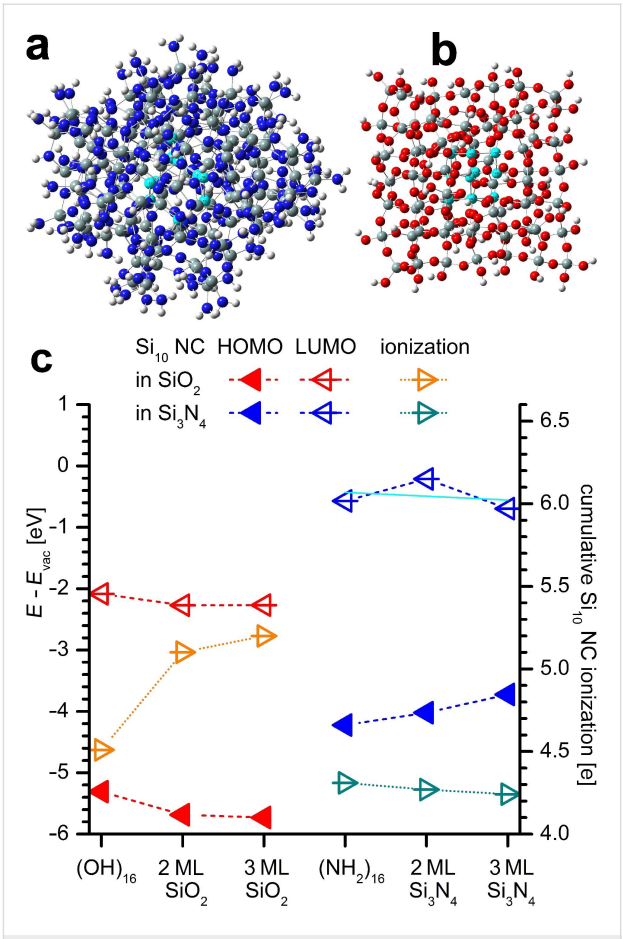



**Figure 2:** Evolution of energy offsets for $SiO_2$- and $Si_3N_4$-embedded $Si_{10}$-NCs (0.8 nm size) as a function of embedding $SiO_2$- or $Si_3N_4$-thickness: (a) $Si_{10}$-NC embedded in 3 ML $Si_3N_4$ after structural optimization. (b) $Si_{10}$-NC embedded in 3 ML $SiO_2$ after structural optimization. For atoms colors see Figure 1. (c) Evolution of HOMO and LUMO energies relative to vacuum energy $E_{vac}$ (left scale) and total $Si_{10}$-NC ionization (right scale) with increasing thickness of embedding dielectric. For $SiO_2$-embedding, the ICT and the associated shift in HOMO and LUMO energies away from $E_{vac}$ saturate quickly. For $Si_3N_4$-embedding, the HOMO energy shifts towards $E_{vac}$. The LUMO energy shift varies around a constant value as shown by a linear fit to LUMO energies (cyan line) as a function of $Si_3N_4$ thickness. The positive NC ionization remains nearly unchanged. These features are due to the positive electron affinity $X$ and the anionic nature of N, resulting in electron delocalization from the NC (ionization) without strong electron localization at N as is the case for O.

Both anions, N and O, dominate electronic bonds to Si by delocalizing a substantial partition of Si valence electrons to form strong polar bonds [13], giving rise to ICT from usn-Si into the respective dielectric ($SiO_2$, $Si_3N_4$) [14]. A high ionicity of bond (IOB) and strong negative electron affinity ($X$) of O result in a strong localization of Si-NC valence electrons. This localization corresponds to increased binding energies – the ICT shifts all MOs away from $E_{vac}$. N is the only anionic element with a positive $X$ [29] which is key for $\Delta E$ together with the smaller IOB of N to Si. Unlike O, the valence electrons delocalized from Si-NCs are *not* strongly localized at N due to its positive $X$

and lower IOB to Si. Such delocalized MOs correspond to states with substantially lowered binding energy, yielding to a shift of MOs towards $E_{vac}$. Accordingly, frontier-MOs of the $Si_3N_4$-embedded NC (Figure 1, insets i and iii) show stronger delocalization as compared to frontier-MOs of the $SiO_2$-embedded Si-NC (Figure 1, inset ii and iv).

Table 1 summarizes the specific properties of Si, O and N relevant to the nature of ICT. The larger bond length of Si–N as compared to Si–O arguably contributes to electron delocalization, while the lower packing fraction of $SiO_2$ is irrelevant in this respect due to strong electron localization at O. Both anions possess about the same ionization due to their IOB to Si together with N and O being trivalent and divalent, respectively. This finding is supported by the virtually identical NC ionization energy of fully $NH_2$- vs OH-terminated Si-NCs (see Supporting Information File 1).

**Table 1:** Fundamental properties of N, O and Si: Ionization energy ($E_{ion}$), electron affinity ($X$), electronegativity (EN), ensuing ionicity of bond (IOB) to Si and experimental values of characteristic bond lengths [29]. See also to Supporting Information File 1 for the latter.

| element | $E_{ion}$[a] [eV] | $X$ [eV] | EN[b] | IOB to Si [%] | $d_{bond}$ to Si [nm] |
|---|---|---|---|---|---|
| N | 14.53 | +0.07 | 3.07 | 36 | 0.1743 ($Si_3N_4$) |
| O | 13.36 | −1.46 | 3.50 | 54 | 0.1626 ($SiO_2$) |
| Si | 8.15 | −2.08 | 1.74 | 0 | 0.2387 (bulk Si)[c] |

[a]Refers to first valence electron.
[b]Values after Allred and Rochow.
[c]With unit cell length of 0.5431 nm [30].

As will be shown experimentally in the next section, the resulting $\Delta E$ of the frontier-MOs induces an n-type (p-type) behaviour in usn-Si by $SiO_2$-embedding ($Si_3N_4$-embedding). For the ICT, and thus the intensity of p- or n-type behaviour, the ratio of interface bonds to atoms forming the Si-NWell, -NWire or -NC is an important parameter [31]. It describes the amount of entities (Si atoms) to be ionized over a certain amount of transfer paths (interface bonds) and depends on the interface facet orientation of the usn-Si volume as well as on its surface-to-volume ratio.

## Sample characterization: TEM and synchrotron-based long-term UPS

We experimentally verified our theoretical findings by characterizing samples comprising 1.7 nm and 2.6 nm thick Si-NWells embedded in $SiO_2$ or $Si_3N_4$ together with a Si reference sample (Figure 3a–d) using synchrotron UPS.

Figure 4a–c shows high-resolution cross-section TEM images of each NWell sample. Such ultrathin Si layers require long

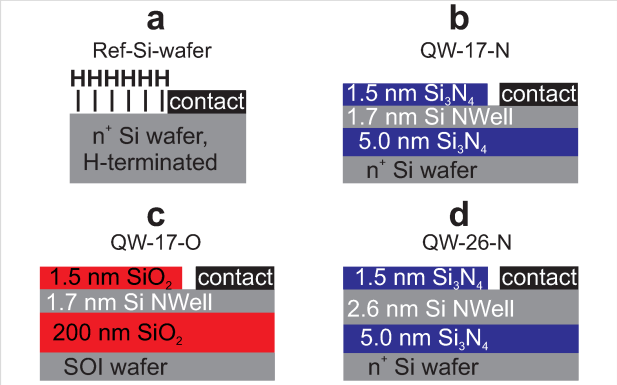



**Figure 3:** Structures of samples investigated by synchrotron UPS: (a) Si-reference, (b) 1.7 nm Si-NWell in $Si_3N_4$, (c) 1.7 nm Si-NWell in $SiO_2$, (d) 2.6 nm Si-NWell in $Si_3N_4$. Sample codes are shown on top of each structure.

signal acquisition times in UPS due to the short mean free path of valence electrons excited above $E_{vac}$[32] in compound with the small Si-volume probed. This is in particular true for

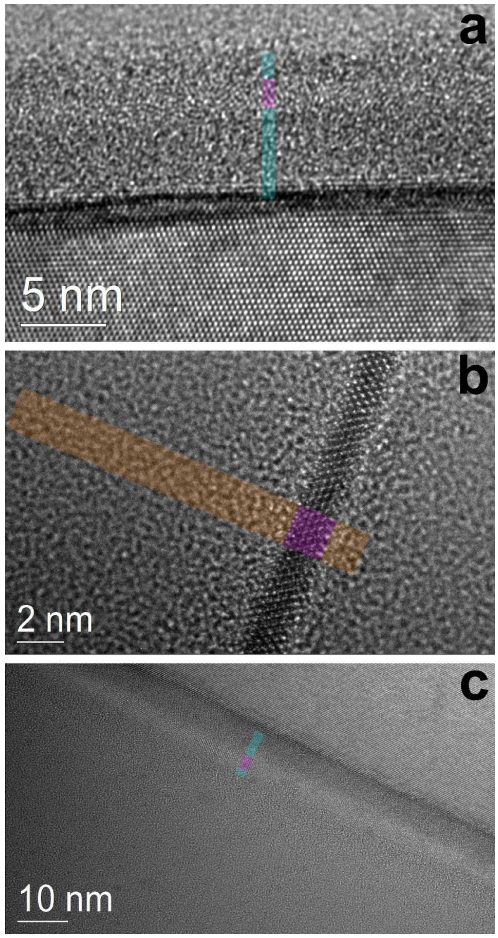



**Figure 4:** Cross-section HR-TEM images of samples QW-17-N (a), QW-17-O (b) and QW-26-N (c). Semi-transparent strips show layer thicknesses of $Si_3N_4$ (cyan), Si-NWells (magenta) and $SiO_2$ (orange).

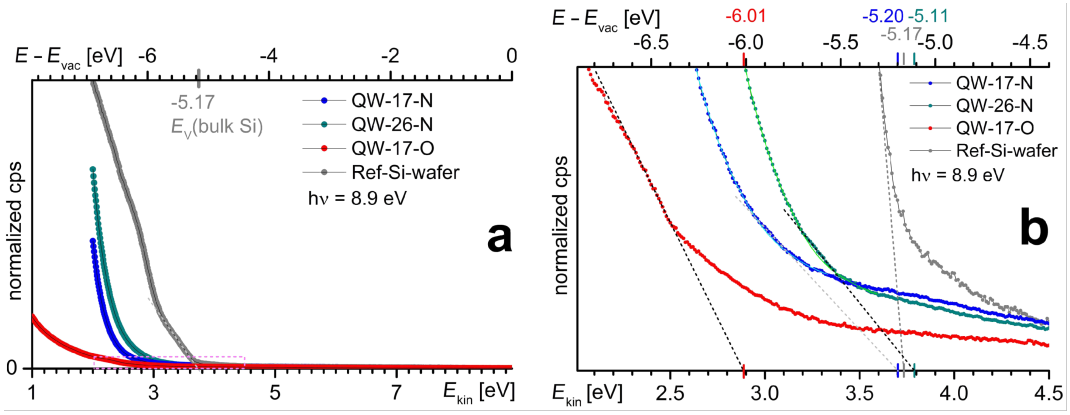



**Figure 5:** Experimental evidence of HOMO Δ*E* by synchrotron UPS: (a) scans of NWell samples and a hydrogen-terminated (111) Si wafer as a reference for the Si-NWells. The valence band edges of Si-NWells detected are located within the magenta lines and shown in (b). The bottom energy scales refer to electron kinetic energy up to UV photon energy. The top energy scale shows the energetic position of electrons relative to vacuum level with valence band edges and respective energy values as extracted from the spectra (dashed lines). The light green and cyan lines show the background fit of the amorphous $Si_3N_4$-matrix. The lower signal-to-noise ratio for Si-NWells embedded in $Si_3N_4$ as compared to $SiO_2$ is comprehensively evaluated and discussed in Supporting Information File 1.

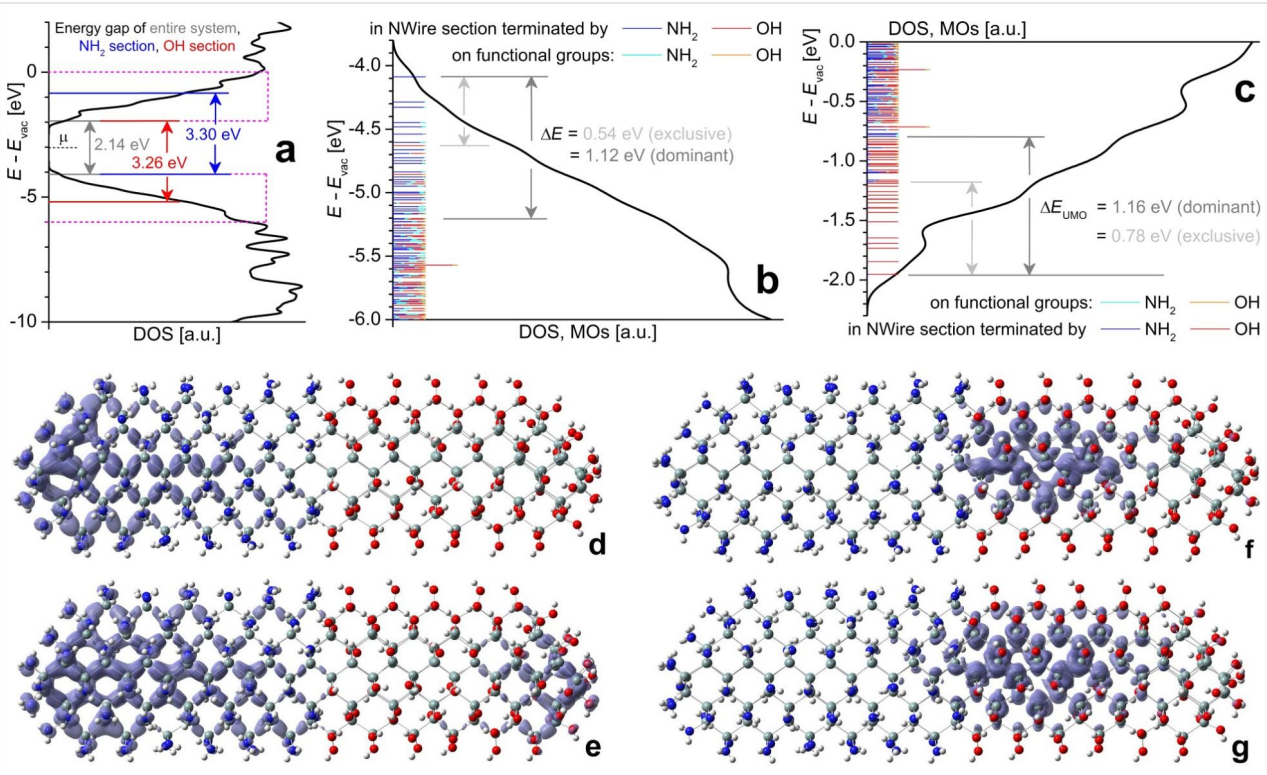



**Figure 6:** Electronic properties obtained by h-DFT for $Si_{233}(NH_2)_{87}(OH)_{81}$ NWire of 1.4 nm diameter and 5.2 nm length, terminated with $NH_2$ on its left half emulating $Si_3N_4$-embedding and with OH on its right half emulating $SiO_2$-embedding: (a) DOS over energy relative to vacuum level $E_{vac}$. Red (blue) lines show HOMO–LUMO-gap of OH-terminated ($NH_2$-terminated) NWire section. Global HOMO–LUMO gap shown in grey together with Fermi energy $E_F$ for entire NWire. Magenta DOS sections are enlarged to show MO locations for (b) frontier-OMOs and (c) frontier-UMOs along with Δ*E* for exclusive and dominant MO location in the respective NWire section. (d–g) $Si_{233}(NH_2)_{87}(OH)_{81}$ approximant after structural optimization; for atom colours see Figure 1. The approximant is shown with the sum of frontier-MO densities $\rho_{MO} = \sum\langle\Psi_{MO}|\Psi^*_{MO}\rangle$ as iso-density plots for: (d) frontier-OMOs exclusively located in the $NH_2$-terminated NWire section ($\rho_{MO} = 1 \times 10^{-3}$ states/$a_0^3$ = 6.76 states/nm$^3$), (e) frontier-OMOs dominantly located in the $NH_2$-terminated NWire section ($\rho_{MO} = 3 \times 10^{-3}$ states/$a_0^3$ = 20.3 states/nm$^3$). A slight distortion of atomic positions occurs at the OH-terminated end due to electrostatic forces, leading to a minor location of MOs otherwise exclusively residing in the $NH_2$-terminated NWire section. This effect does not occur at NWire devices where $SiO_2$ coverage is followed by a contact layer, see Figure 7. (f) Frontier-UMOs exclusively located in the OH-terminated NWire section ($\rho_{MO} = 2 \times 10^{-3}$ states/$a_0^3$ = 13.5 states/nm$^3$), and (g) frontier-UMOs dominantly located in the OH-terminated NWire section ($\rho_{MO} = 3 \times 10^{-3}$ states/$a_0^3$ = 20.3 states/nm$^3$). Values for $\rho_{MO}$ are scaled to provide $\rho_{MO} = 1 \times 10^{-4}$ states/$a_0^3$ = 0.675 states/nm$^3$ per MO.

Si-NWells embedded in $Si_3N_4$ as discussed in Supporting Information File 1.

UPS spectra are shown in Figure 5. The reference sample (Si-ref) yielded a valence band edge at the ionization energy $E_{ion} = E_{vac} - 5.17$ eV as known for bulk Si [33]. We obtained $E_{ion} = E_{vac} - 6.01$ eV for the 1.7 nm Si-NWell in $SiO_2$ and $E_{ion} = E_{vac} - 5.20$ eV ($E_{vac} - 5.11$ eV) for the 1.7 (2.6) nm Si-NWell in $Si_3N_4$. The difference in ionization energy $\Delta E_{ion}$ between 1.7 nm Si-NWells in $SiO_2$ and $Si_3N_4$ is 0.81 eV which clearly confirms our h-DFT calculations. For the 2.6 nm NWell embedded in $Si_3N_4$ we obtain a $E_{ion}$ of 0.06 eV below the value of bulk Si (Figure 5b). The ICT may thus overcompensate quantum confinement and induce a negative $\Delta E_{ion}$ to bulk Si. The ICT impact length on Si-NWells can be related to Si-NWires and Si-NCs to scale 1/2/3 for NWells/NWires/NCs [14]. This relation explains why larger $\Delta E$ values for HOMOs and LUMOs are obtained for Si-NWires (Figure 6) as compared to Si-NWells (Figure 5b).

## Concept of undoped Si nanowire FETs

With the $\Delta E$ values of the usn-Si coated with $SiO_2$ vs $Si_3N_4$ confirmed by synchrotron UPS, we now turn to its application to undoped ULSI Si devices.

NWire-FETs are a cornerstone of future ULSI technology development due to their excellent controllability by wrap-around gate architecture [34,35]. However, the ultrasmall NWire diameter required to guarantee the electrostatic integrity of the devices causes conventional doping to fail. Metal–Si contacts formed by, e.g., silicide formation [36] result in rather high Schottky-barriers at the source/drain-channel interfaces that deteriorate the switching behaviour and on-state performance.

## h-DFT calculations of Si nanowires relevant to devices

As we will show below, a Si-NWire with a combined $SiO_2$-/$Si_3N_4$-coating can work as a highly scalable, high-performance and dopant-free metal-insulator-silicon (MIS) FET device. Using the same h-DFT methods as above, we computed the electronic properties of a $Si_{233}(NH_2)_{87}(OH)_{81}$ approximant manifesting a Si-NWire with 1.4 nm diameter and 5.2 nm length, whereby the two halves of this NWire are terminated with $NH_2$ and OH groups, respectively. These functional groups correspond to 1 ML of the respective dielectric – $NH_2$ groups to 1 ML $Si_3N_4$ and OH groups to 1 ML $SiO_2$ (Figure 6).

Figure 6a shows the DOS around the HOMO–LUMO gap. We determined the location of the densities of all frontier-MOs, $\rho_{MO} = \langle \Psi_{MO} | \Psi^*_{MO} \rangle$, within 2 eV from HOMO and LUMO. Frontier-OMOs are located within the $NH_2$-terminated NWire section with a $\Delta E$ to corresponding MOs in the OH-terminated NWire section of ≈1.1 eV. Frontier-UMOs exist in the OH-terminated NWire section, whereby $\Delta E$ from the OH- to $NH_2$-terminated NWire section is ≈1.2 eV. Again, the increased values of $\Delta E$ of respective frontier-MOs as compared to UPS results of Si-NWells confirm geometric effects [14].

## Undoped Si-NWire FETs

The electronic structure of the $Si_{233}(NH_2)_{87}(OH)_{81}$ NWire allows $\Delta E$ values to be established for NWire electronic devices with a combined $SiO_2$-/$Si_3N_4$-coating such as an undoped self-blocking p-channel FET (Figure 7).

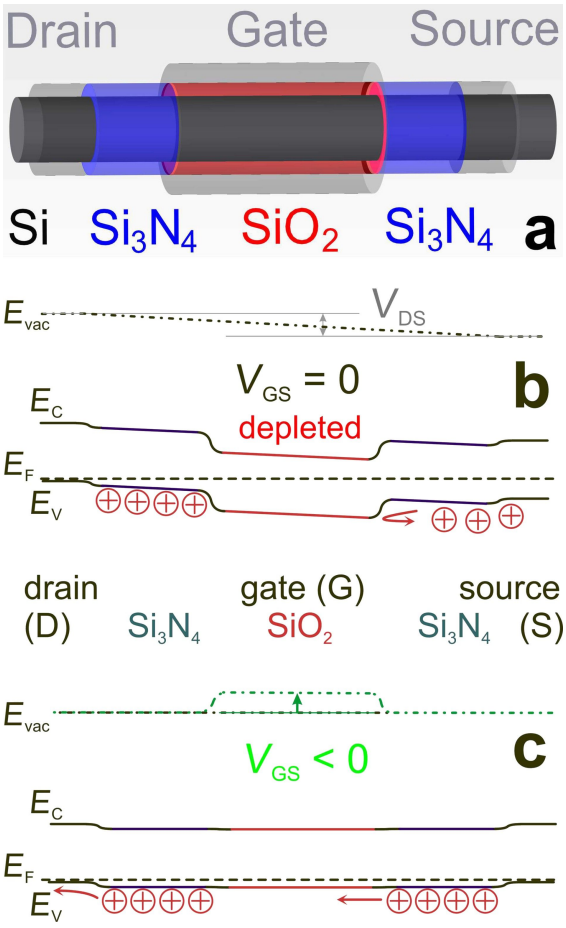



**Figure 7:** Concept of an undoped FET consisting of a Si-NWire with drain/gate (channel)/source regions covered by ultrathin $Si_3N_4$/$SiO_2$/$Si_3N_4$: (a) physical layout shown for self-blocking p-channel FET. Schematic band diagram of such an FET shown for (b) zero and (c) negative gate bias relative to source voltage, resulting in a conductive channel by shifting the electronic Si-NWire states pinned by $SiO_2$. Interchanging $Si_3N_4$ and $SiO_2$ layers yields self-blocking n-channel FETs and thereby CMOS-compatibility. This concept is applicable to other Si nanostructures with a high surface-to-volume ratio like fin-FETs.

Using the $\Delta E$ value obtained from the $Si_{233}(NH_2)_{87}(OH)_{81}$ NWire approximant and above-described UPS results,

we derive hole ($p$) and electron ($n$) densities. We obtain $p = 5 \times 10^{19}$ cm$^{-3}$ ($n \approx 0$ cm$^{-3}$) for the $Si_3N_4$-coated NWire-regions (drain/source) and $p = 71$ cm$^{-3}$ ($n \approx 0$ cm$^{-3}$) for the $SiO_2$-coated NWire-regions (see Supporting Information File 1). These values will be used in the next section where results on NEGF device simulations are presented.

## NEGF device simulations

NEGF simulations were realized considering a 1.7 nm thick undoped Si-NWire MISFET with a channel length of $L = 5$ nm in a wrap-gate architecture placed between two metallic contacts (Figure 8a). The channel is insulated by a $SiO_2$ layer, yielding an effective oxide thickness of 2 nm. The source/drain and the gate electrode are insulated from each other by an underlap region of length $l_{con}$ where the NWire is covered with a 2 nm thick $Si_3N_4$ (device I) or $SiO_2$ (device II) layer, resulting in dopant concentration equivalents as mentioned above. Ni source/drain contacts are considered to yield effective Schottky-barriers of −0.05 eV for hole-injection into the Si-NWire valence band.

Figure 8c shows drain-current versus gate-voltage characteristics of device I and II for an underlap of $l_{con} = 5$ nm. The $SiO_2$ gate insulator yields a built-in potential that results in self-blocking FETs at $V_{GS} = 0$ V. Clearly, device I shows a substantially higher on-state performance, becoming even more obvious with increasing underlap region $l_{con}$. The inset of Figure 8c displays the drive current at $V_{GS} = -1.5$ V, showing that device I exhibits very small current degradation with increasing $l_{con}$ due to effective "doping" ($Si_3N_4$-coating) within the underlap region. In contrast, device II strongly depends on $l_{con}$ with substantial drive current degradation if $l_{con}$ increases. Device II only delivers an acceptable performance for $l_{con} < 5$ nm which ensues a very large parasitic capacitance and presents a challenge to ULSI processing. Moreover, any variation in $l_{con}$ translates into a strong variability of drive current. This massive deterioration of device II is caused by the lack of "doping", yielding a substantial increase in potential barriers (cf. Figure 8b) in particular at the gate-channel/gate-underlap interface and at the Ni–contact–Si interfaces, both depending on $l_{con}$ (see Supporting Information File 1). Without the energy shift caused by $Si_3N_4$-coatings in source/drain, we obtain substantially higher Schottky-barriers for device II, resulting in severely deteriorated device performance. Our simulations underline the great importance of alternatives to conventional doping for increased performance of future ULSI transistors.

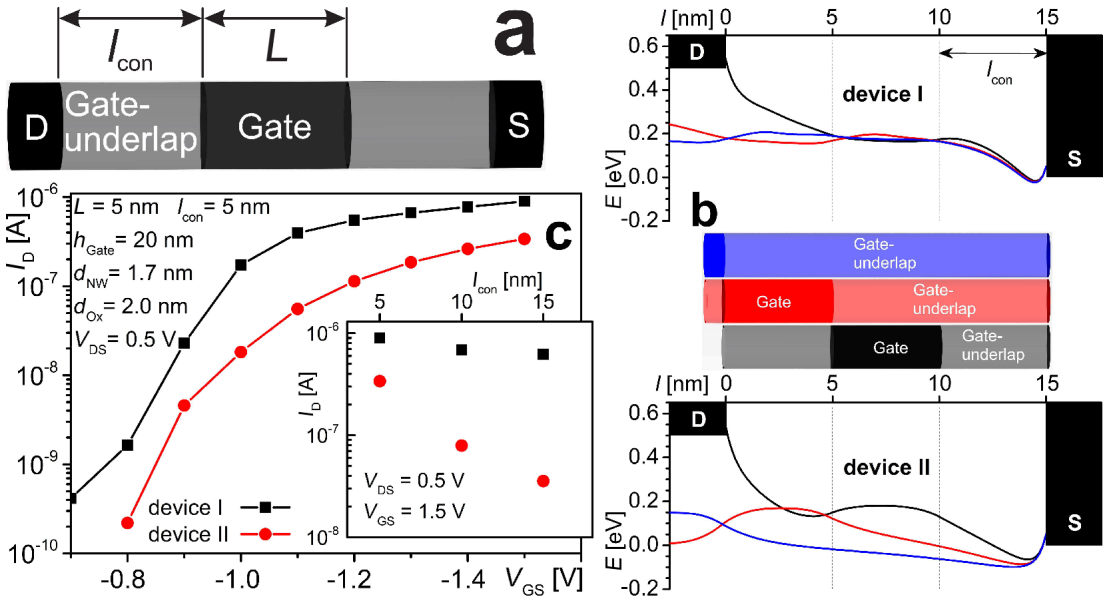



**Figure 8:** NEGF simulation results of undoped Si-NWire-FET illustrated in Figure 7: (a) gate-wrap-around Si-NWire FET showing parameters listed in graphs (b) and (c). (b) Valence band along the axis of device I (top, $Si_3N_4$-coated gate-underlap) and device II Si-NWire FET (bottom, entire Si-NWire $SiO_2$-coated) in on-state-mode with $V_{GS} = -1.2$ V. The centre schematic shows the NWire-FET device gate-position and gate-underlap. Schottky-potential barriers build up although the same Schottky-barrier-height at the metal–Si interface at drain and source were chosen in both devices to examine the effectiveness of "doping" ($Si_3N_4$-coating) of underlap areas. A shift of the Schottky-barrier for device II due to workfunction mismatch of Ni to the valence band of the $SiO_2$-coated Si-NWire would lead to a further massive deterioration of the on-state performance of device II. (c) Transfer characteristics of device type I (black) and II (red) for $V_{DS} = 0.5$ V, contact length $l_{con} = 5$ nm; the graph contains remaining parameters. The "doping" generated via ICT yields a substantially higher on-state performance in device I vs device II (no $Si_3N_4$-coated gate-underlap), an effect that becomes even more significant with increasing contact length $l_{con}$, see inset. Hence, device II has low on-state performance and is prone to variability.

## Conclusion

We demonstrated quantitatively in theory and experiment that the intrinsic electronic properties of usn-Si can yield p- (n-) type behaviour by shifting the electronic DOS towards (away from) $E_{vac}$ using ultrathin $Si_3N_4$- ($SiO_2$-) coatings. The key parameters for this phenomenon are the electron affinities $X$ of N and O together with their IOB and bond length to Si. Using NEGF device simulations we compared two undoped Si-NWire-FETs with $SiO_2$- or $Si_3N_4$-coating in the source/drain regions and $SiO_2$-coated gate area. We demonstrated that devices with $Si_3N_4$-coating exhibit substantially better on-state performance and strongly reduced dependence on the length of the source/drain regions, showing that high performance small-scale MISFETs can be realized using undoped ultrathin Si-NWires with a combined $SiO_2$-/$Si_3N_4$-coating. Our findings open a whole new vista on Si-based ULSI operating at lower voltages and lower heat loss. Doping-related technological obstacles typical in CMOS technology are bypassed altogether, extending the potential of structural miniaturization down to the Si-crystallization limit of ca. 1.5 nm [15].

## Supporting Information

Supporting Information features the comparison of h-DFT results to experimental data, further information on the interface impact on Si nanocrystal electronic structure and its connection to quantum-chemical nature of N and O, details of UPS scans with further reference data, the derivation of charge carrier densities for nonequilibrium Green's function (NEGF) transport simulation of undoped Si-nanowire MISFET devices and details on NEGF device simulations.

### Supporting Information File 1

Further discussion and data of h-DFT, UPS, and NEGF simulations.
[https://www.beilstein-journals.org/bjnano/content/supplementary/2190-4286-9-210-S1.pdf]

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